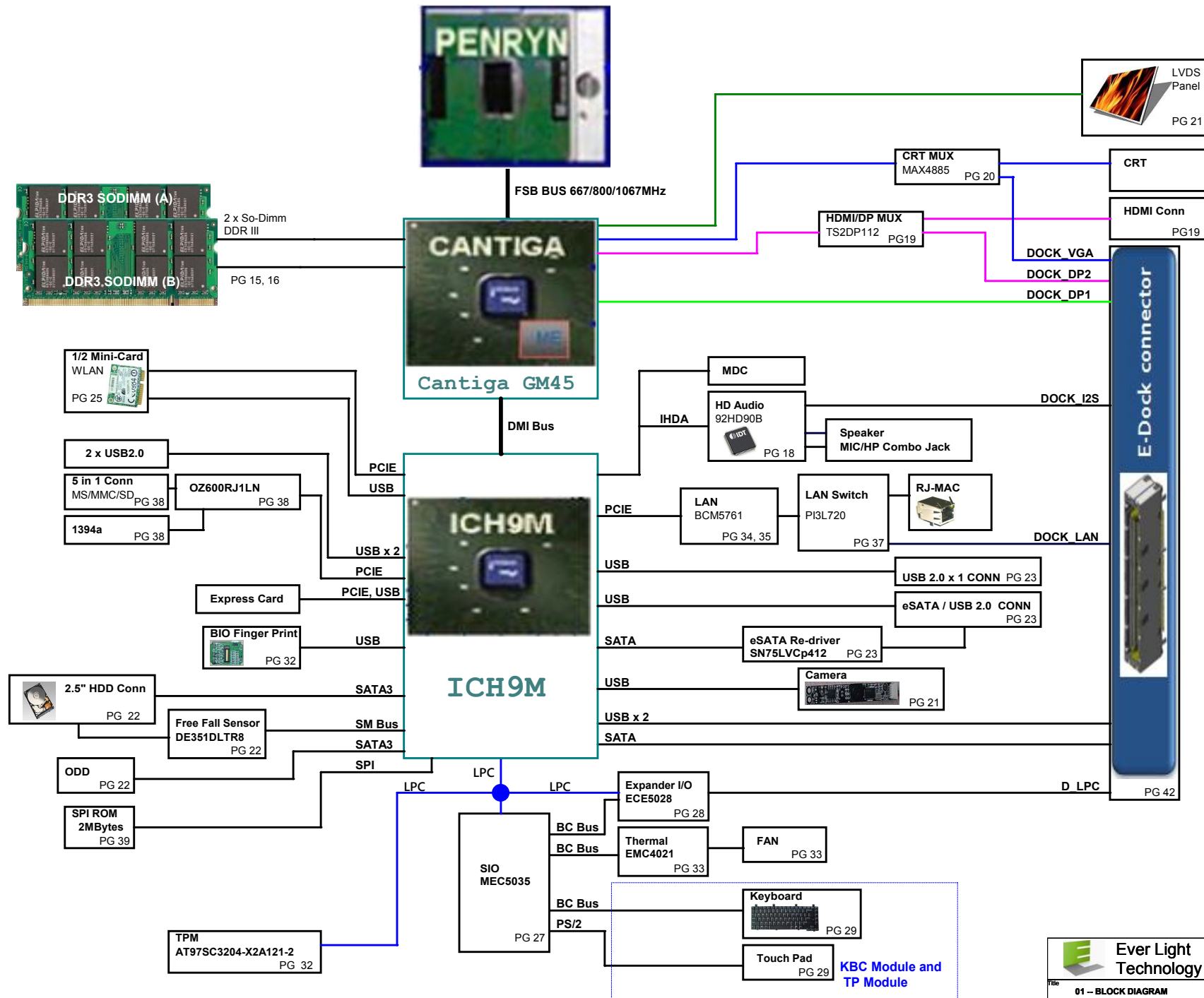
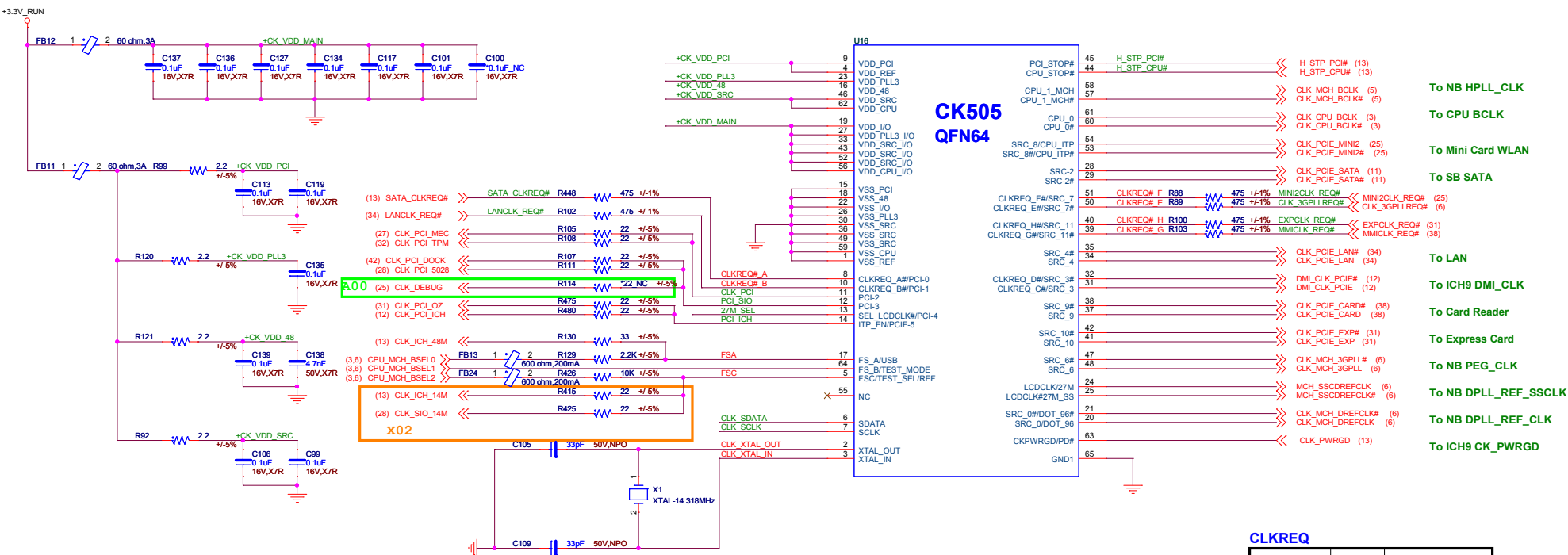


# B3 Montevina 14 UMA Block Diagram

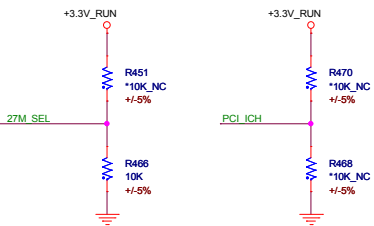


CLOCK GEN



BSEL Frequency Select Table

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
0	0	0	266M	1066M
0	0	1	133M	X
0	1	0	200M	800M
0	1	1	166M	X



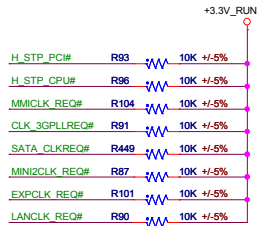
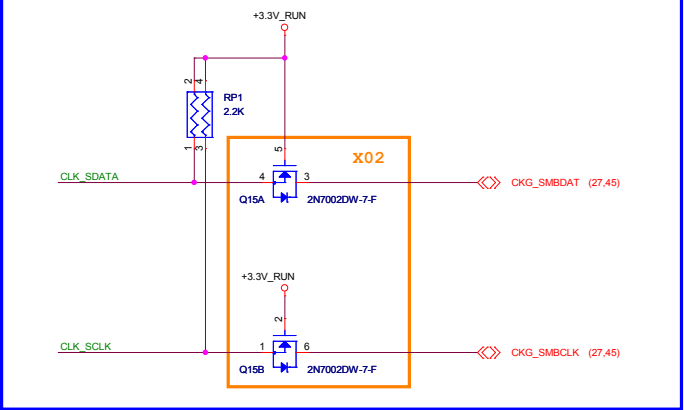
27M\_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

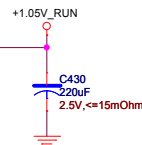
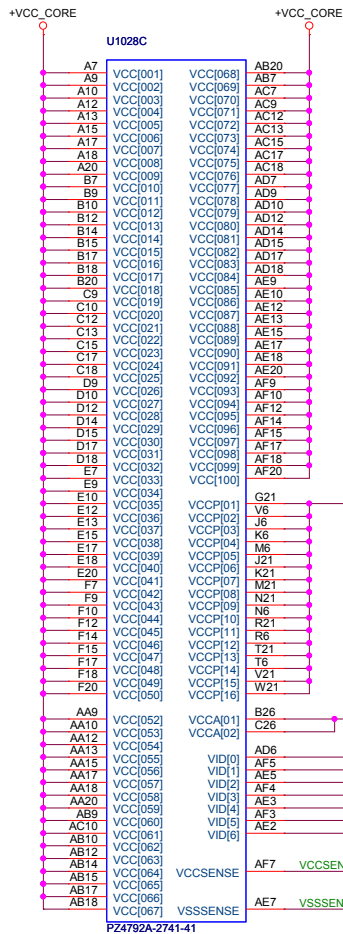
CLKREQ

CLKREQ_A	SRC2	SATA
CLKREQ_B	SRC4	LAN
CLKREQ_E	SRC6	NB PEG_CLK
CLKREQ_F	SRC8	WLAN MiniCard
CLKREQ_G	SRC9	Card Reader
CLKREQ_H	SRC10	Express Card

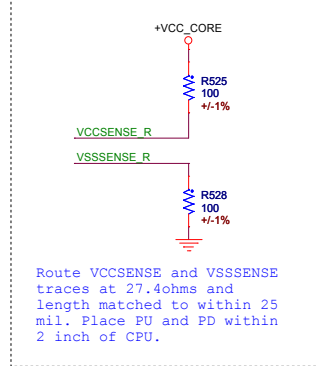
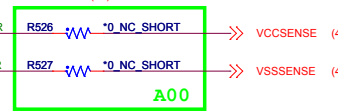
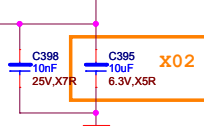
SMBus address D2



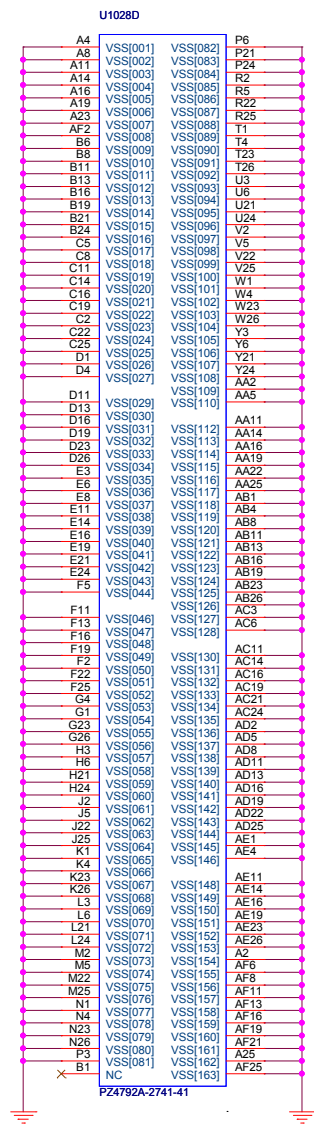
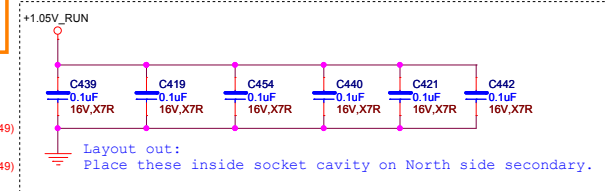
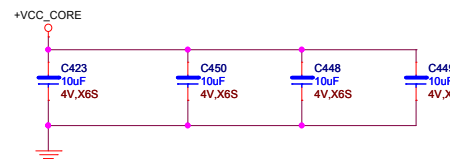
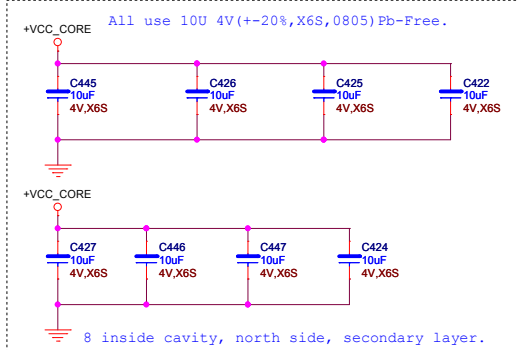




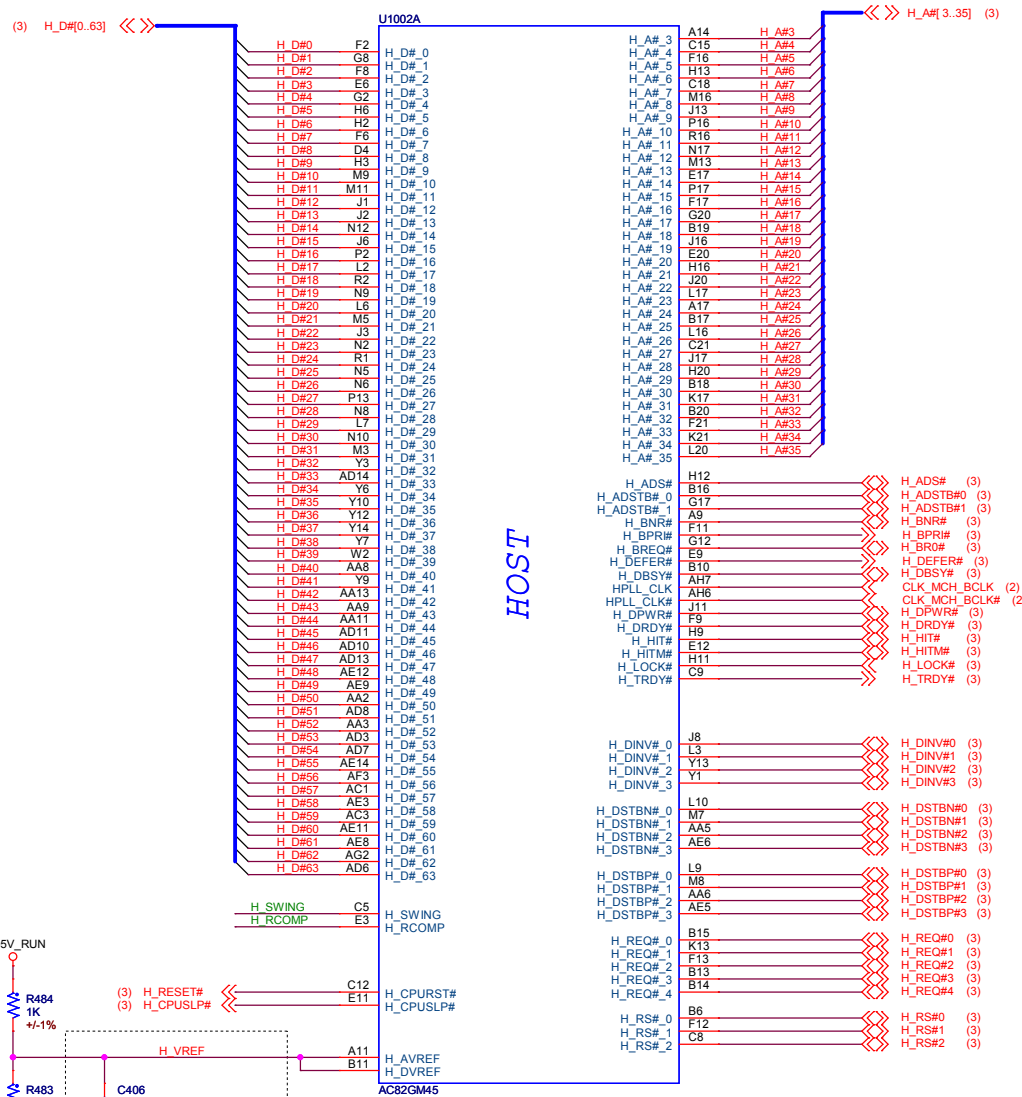
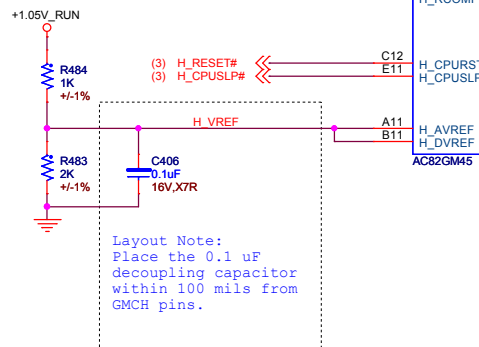
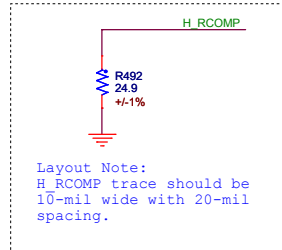
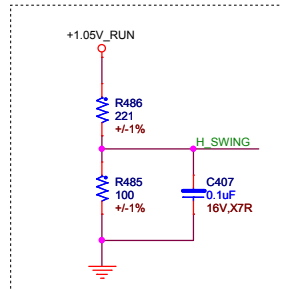
+1.5V\_RUN



Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.



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# Vinafix

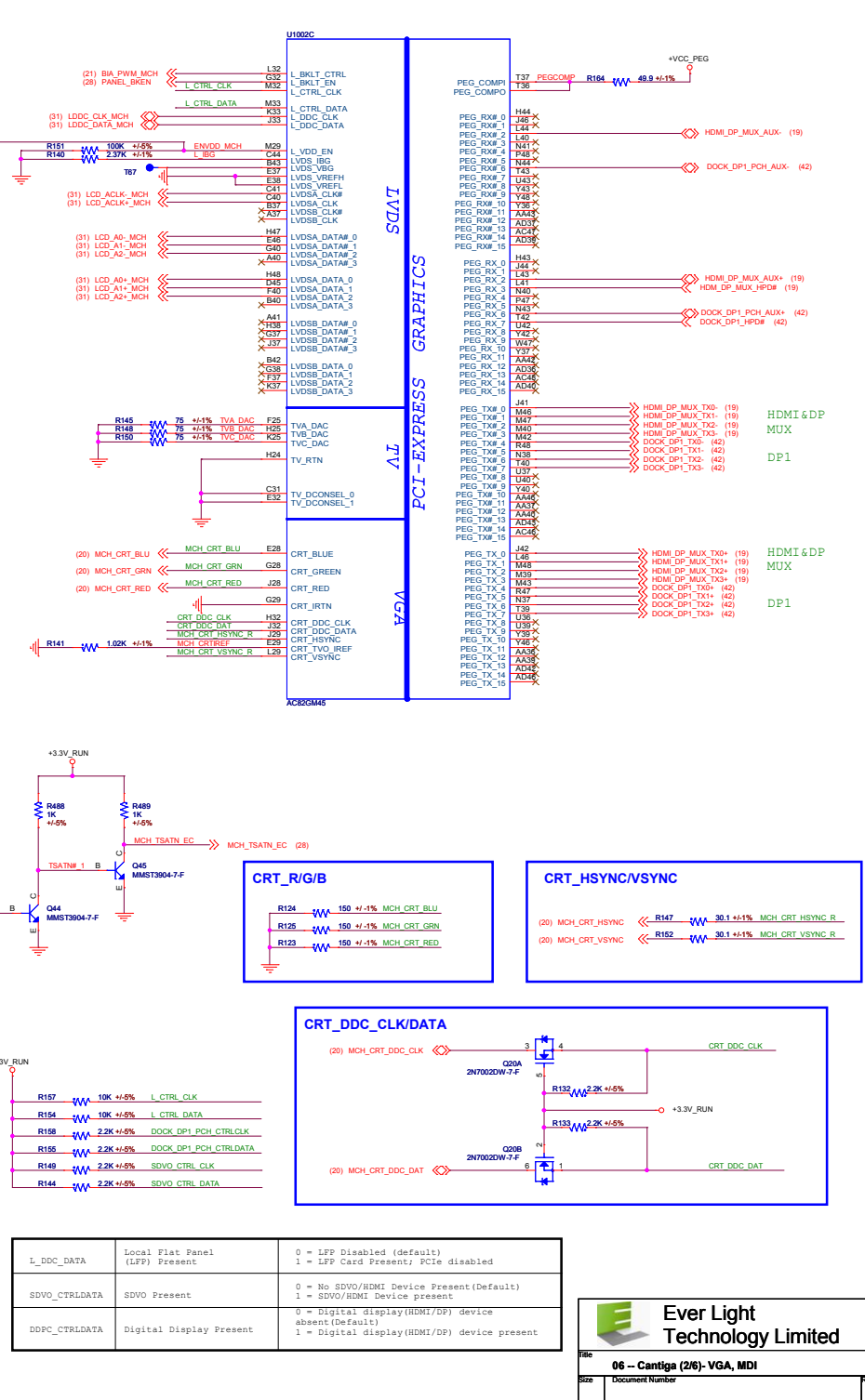
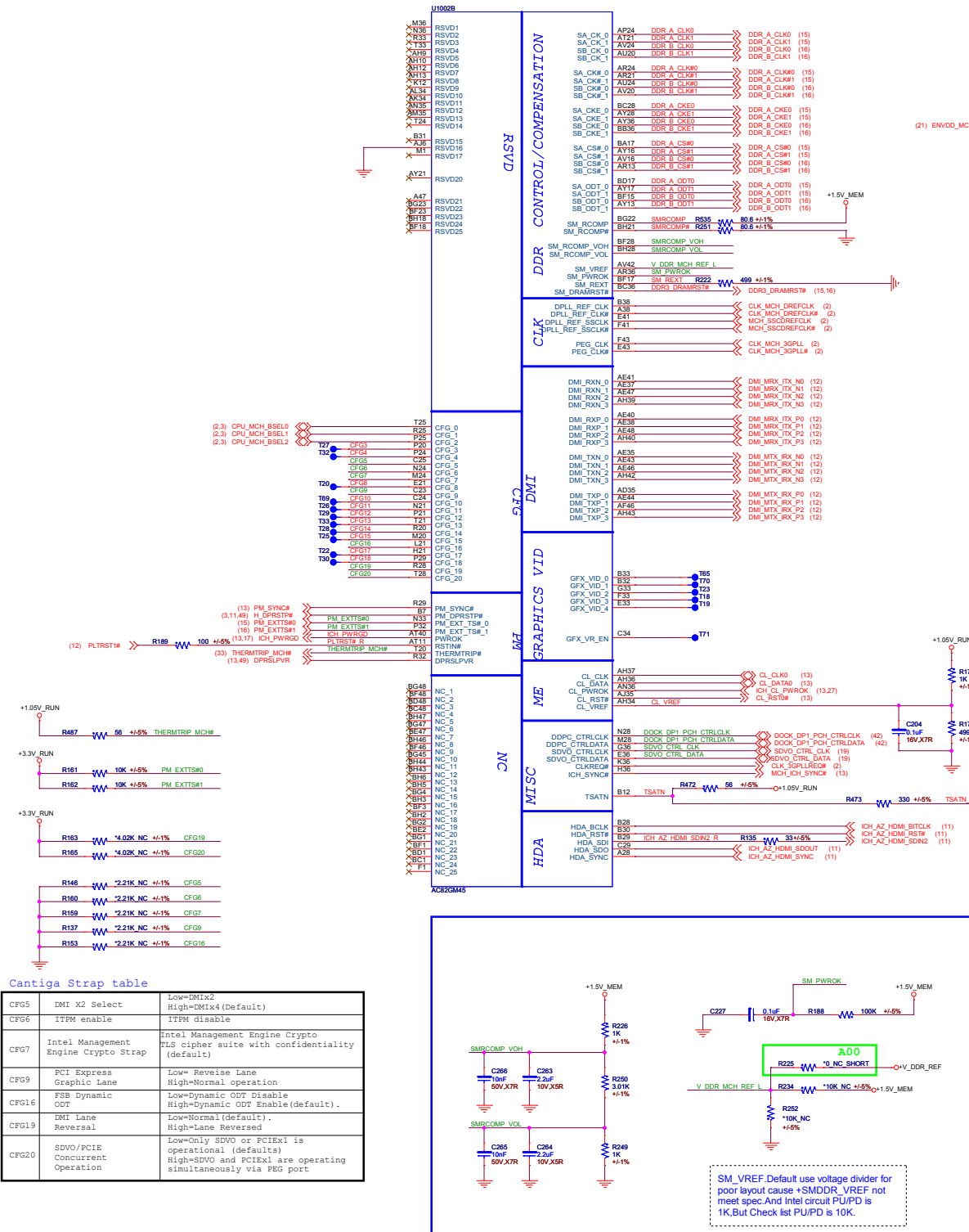


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Title		
05 -- Cantiga (1/6)- HOST		
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Cantiga Strap table

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG6	ITPM enable	ITPM disable
CFG7	Intel Management Engine Crypto Strap	Intel Management Engine Crypto R15 cipher suite with confidentiality (default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe1 are operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port



L_DOC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (default) 1 = LFP Card Present; PCIe disabled
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display (HDMI/DP) device absent(Default) 1 = Digital display (HDMI/DP) device present



(15) DDR\_A\_D[0..63] <<<

DDR A D0	AJ38	SA_DQ_0
DDR A D1	AJ41	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	AJ36	SA_DQ_4
DDR A D5	AJ40	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AU40	SA_DQ_10
DDR A D11	AT38	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AU44	SA_DQ_14
DDR A D15	AU42	SA_DQ_15
DDR A D16	AV39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BB41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AY38	SA_DQ_28
DDR A D29	BB38	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AU11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AU13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BB9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AU10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AU5	SA_DQ_52
DDR A D53	AU6	SA_DQ_53
DDR A D54	AT5	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	AJ9	SA_DQ_58
DDR A D59	AJ8	SA_DQ_59
DDR A D60	AN12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0
SA_BS_1	BC18	DDR A BS1
SA_BS_2	AT25	DDR A BS2
SA_RAS#	BB20	DDR A RAS#
SA_CAS#	BD20	DDR A CAS#
SA_WE#	AY20	DDR A WE#
SA_DM_0	AM37	DDR A DM0
SA_DM_1	AY41	DDR A DM2
SA_DM_2	AU39	DDR A DM3
SA_DM_3	BB12	DDR A DM4
SA_DM_4	AY6	DDR A DM5
SA_DM_5	AT17	DDR A DM6
SA_DM_6	AJ5	DDR A DM7
SA_DQS_0	AJ44	DDR A DQS0
SA_DQS_1	AT44	DDR A DQS1
SA_DQS_2	BA43	DDR A DQS2
SA_DQS_3	BC37	DDR A DQS3
SA_DQS_4	AW12	DDR A DQS4
SA_DQS_5	BC8	DDR A DQS5
SA_DQS_6	AU8	DDR A DQS6
SA_DQS_7	AM7	DDR A DQS7
SA_DQS#_0	AJ43	DDR A DQS#0
SA_DQS#_1	AT43	DDR A DQS#1
SA_DQS#_2	BA44	DDR A DQS#2
SA_DQS#_3	BD37	DDR A DQS#3
SA_DQS#_4	AY12	DDR A DQS#4
SA_DQS#_5	BD8	DDR A DQS#5
SA_DQS#_6	AU9	DDR A DQS#6
SA_DQS#_7	AM8	DDR A DQS#7
SA_MA_0	BA21	DDR A MA0
SA_MA_1	BC24	DDR A MA2
SA_MA_2	BG24	DDR A MA1
SA_MA_3	BH24	DDR A MA3
SA_MA_4	BC25	DDR A MA4
SA_MA_5	BA24	DDR A MA5
SA_MA_6	BD24	DDR A MA6
SA_MA_7	BG27	DDR A MA7
SA_MA_8	BF25	DDR A MA8
SA_MA_9	AW24	DDR A MA9
SA_MA_10	BC21	DDR A MA10
SA_MA_11	BG26	DDR A MA11
SA_MA_12	BH26	DDR A MA12
SA_MA_13	BH17	DDR A MA13
SA_MA_14	AY25	DDR A MA14

DDR\_A\_DM[0..7] (15)

DDR\_A\_DQS[0..7] (15)

DDR\_A\_DQS#[0..7] (15)

DDR\_A\_MA[0..14] (15)

(16) DDR\_B\_D[0..63] <<<

DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	AJ48	SB_DQ_5
DDR B D6	AM48	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AU47	SB_DQ_8
DDR B D9	AU46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	BA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	BC46	SB_DQ_16
DDR B D17	BC44	SB_DQ_17
DDR B D18	BC43	SB_DQ_18
DDR B D19	BF43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BF40	SB_DQ_22
DDR B D23	BC41	SB_DQ_23
DDR B D24	BC38	SB_DQ_24
DDR B D25	BF38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BC39	SB_DQ_29
DDR B D30	BC34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BC8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BF11	SB_DQ_37
DDR B D38	BF8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BF6	SB_DQ_44
DDR B D45	BF5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AU3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	AJ1	SB_DQ_58
DDR B D59	AH1	SB_DQ_59
DDR B D60	AM2	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

SB_BS_0	BC16	DDR B BS0
SB_BS_1	BB17	DDR B BS1
SB_BS_2	BB33	DDR B BS2
SB_RAS#	AU17	DDR B RAS#
SB_CAS#	BG16	DDR B CAS#
SB_WE#	BF14	DDR B WE#
SB_DM_0	AM47	DDR B DM0
SB_DM_1	AY47	DDR B DM1
SB_DM_2	BD40	DDR B DM2
SB_DM_3	BF35	DDR B DM3
SB_DM_4	BG11	DDR B DM4
SB_DM_5	BA3	DDR B DM5
SB_DM_6	AP1	DDR B DM6
SB_DM_7	AK2	DDR B DM7
SB_DQS_0	AL47	DDR B DQS0
SB_DQS_1	AV48	DDR B DQS1
SB_DQS_2	BG41	DDR B DQS2
SB_DQS_3	BG37	DDR B DQS3
SB_DQS_4	BH9	DDR B DQS4
SB_DQS_5	BB2	DDR B DQS5
SB_DQS_6	AU1	DDR B DQS6
SB_DQS_7	AN6	DDR B DQS7
SB_DQS#_0	AL48	DDR B DQS#0
SB_DQS#_1	AV47	DDR B DQS#1
SB_DQS#_2	BH41	DDR B DQS#2
SB_DQS#_3	BH37	DDR B DQS#3
SB_DQS#_4	BG9	DDR B DQS#4
SB_DQS#_5	BC2	DDR B DQS#5
SB_DQS#_6	AT2	DDR B DQS#6
SB_DQS#_7	AN5	DDR B DQS#7
SB_MA_0	AV17	DDR B MA0
SB_MA_1	BA25	DDR B MA1
SB_MA_2	BC25	DDR B MA2
SB_MA_3	AU25	DDR B MA3
SB_MA_4	AW25	DDR B MA4
SB_MA_5	BB28	DDR B MA5
SB_MA_6	AU28	DDR B MA6
SB_MA_7	AW28	DDR B MA7
SB_MA_8	AT33	DDR B MA8
SB_MA_9	BD33	DDR B MA9
SB_MA_10	BB16	DDR B MA10
SB_MA_11	AW33	DDR B MA11
SB_MA_12	AY33	DDR B MA12
SB_MA_13	BH15	DDR B MA13
SB_MA_14	AU33	DDR B MA14

DDR\_B\_DM[0..7] (16)

DDR\_B\_DQS[0..7] (16)

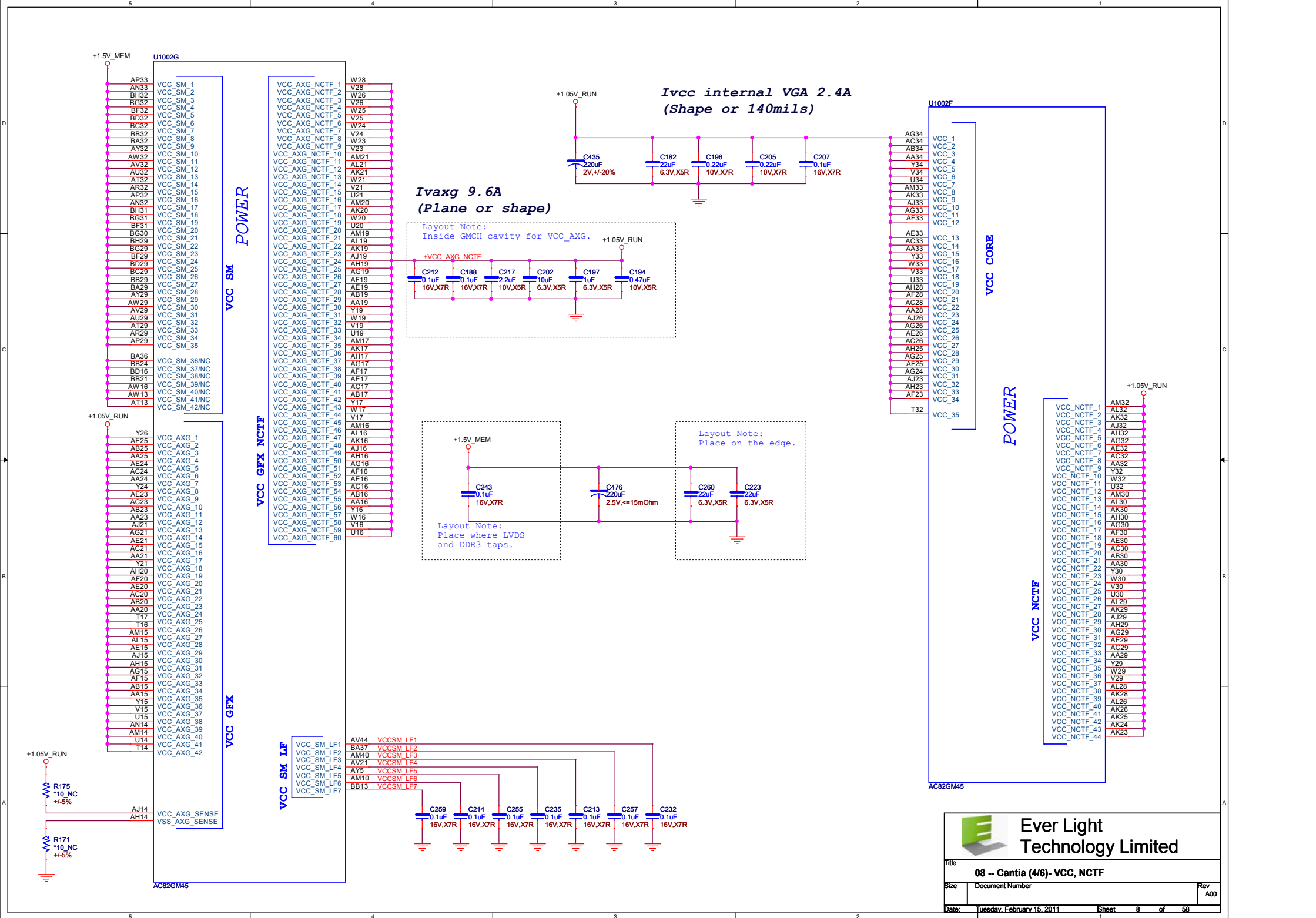
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DDR\_B\_MA[0..14] (16)

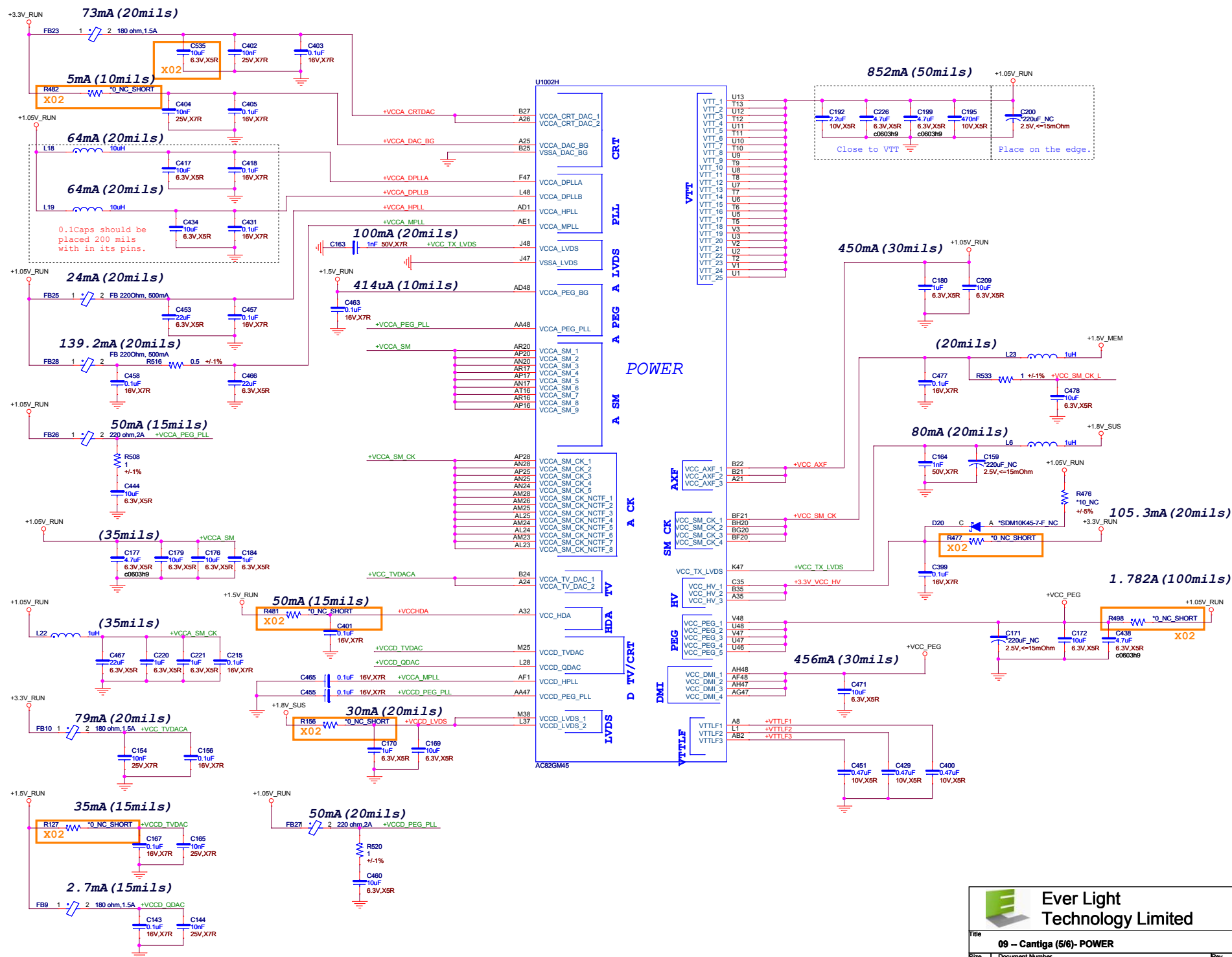


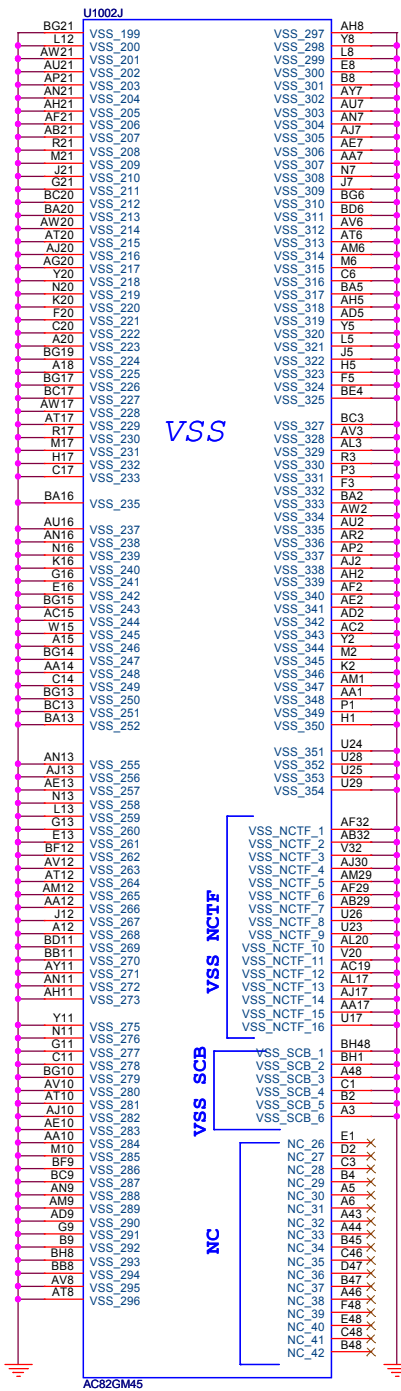
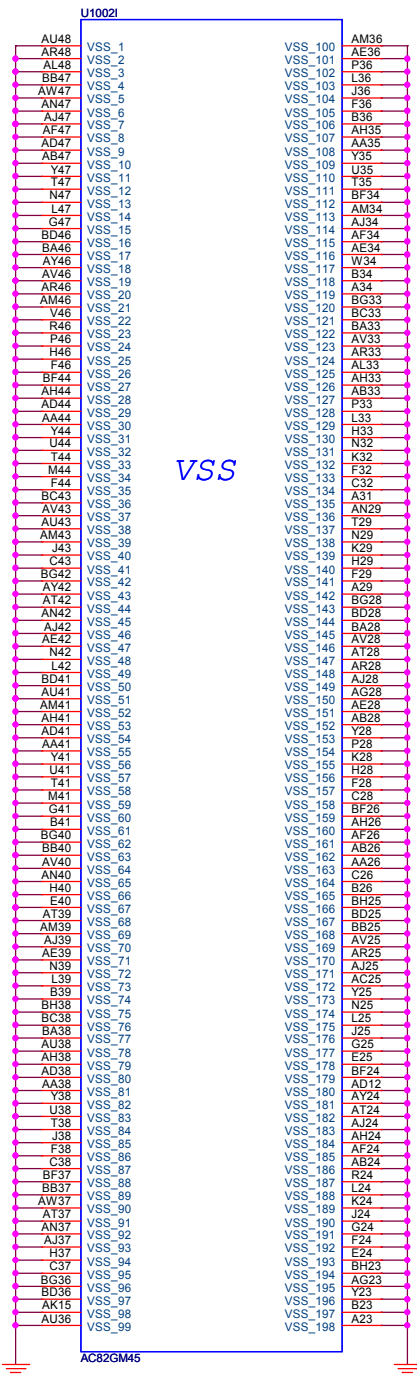
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Title 07 -- Cantiga (3/6)- DDRIII		
Size	Document Number	Rev A00
Date:	Tuesday, February 15, 2011	Sheet 7 of 58

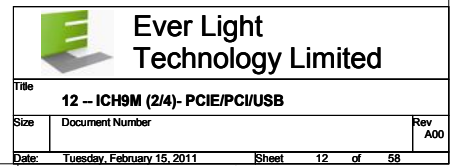


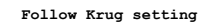




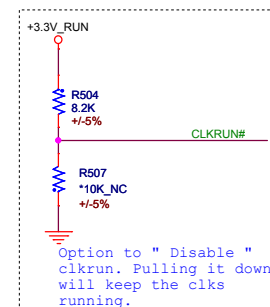
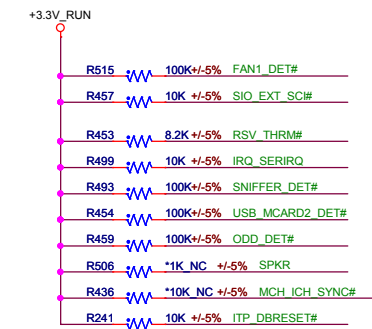






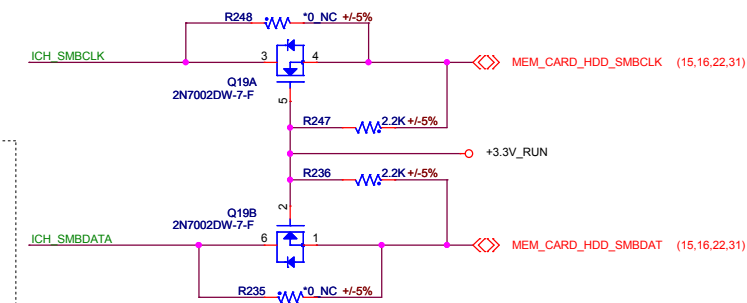
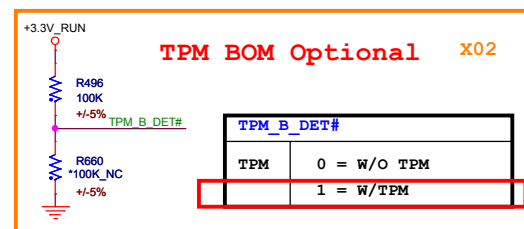
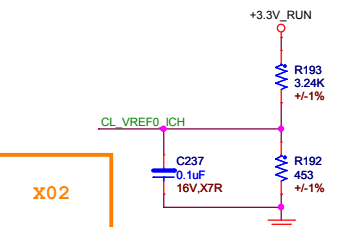
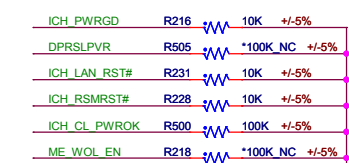
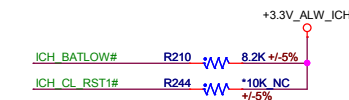
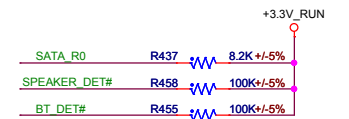
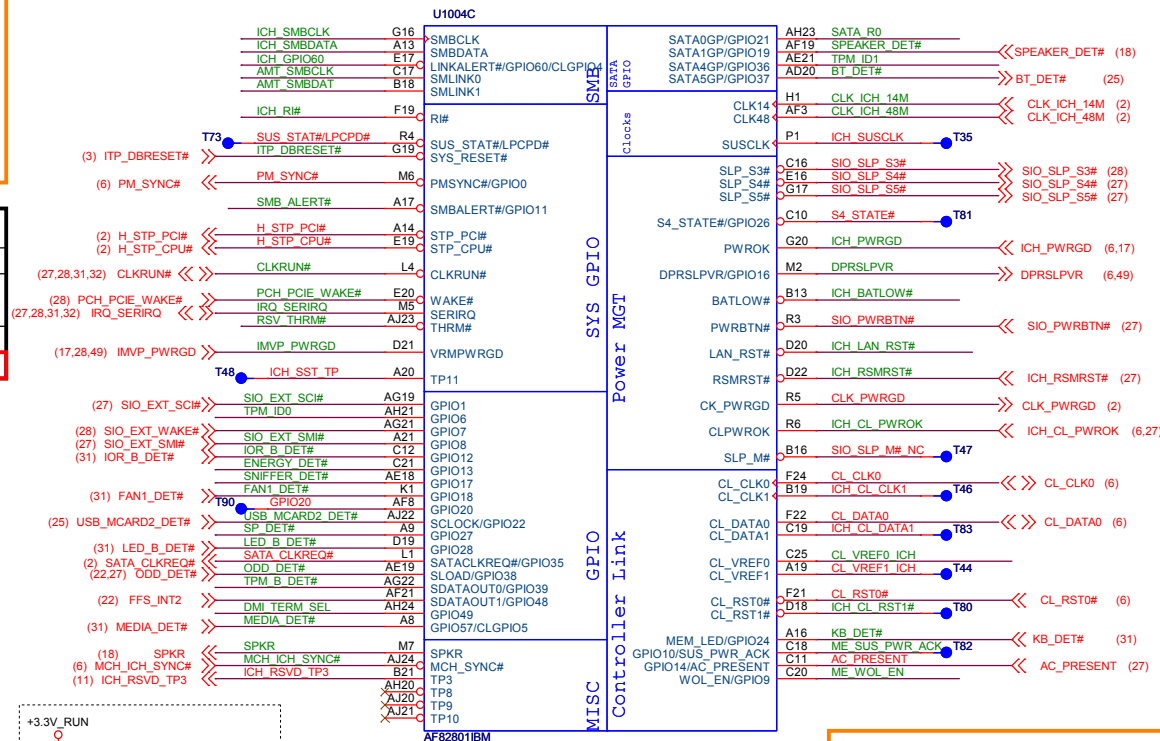


	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	1	0
RSVD	0	1
TPM	1	1



No Reboot Strap	
SPKR	0 = Defaule
	1 = No Reboot

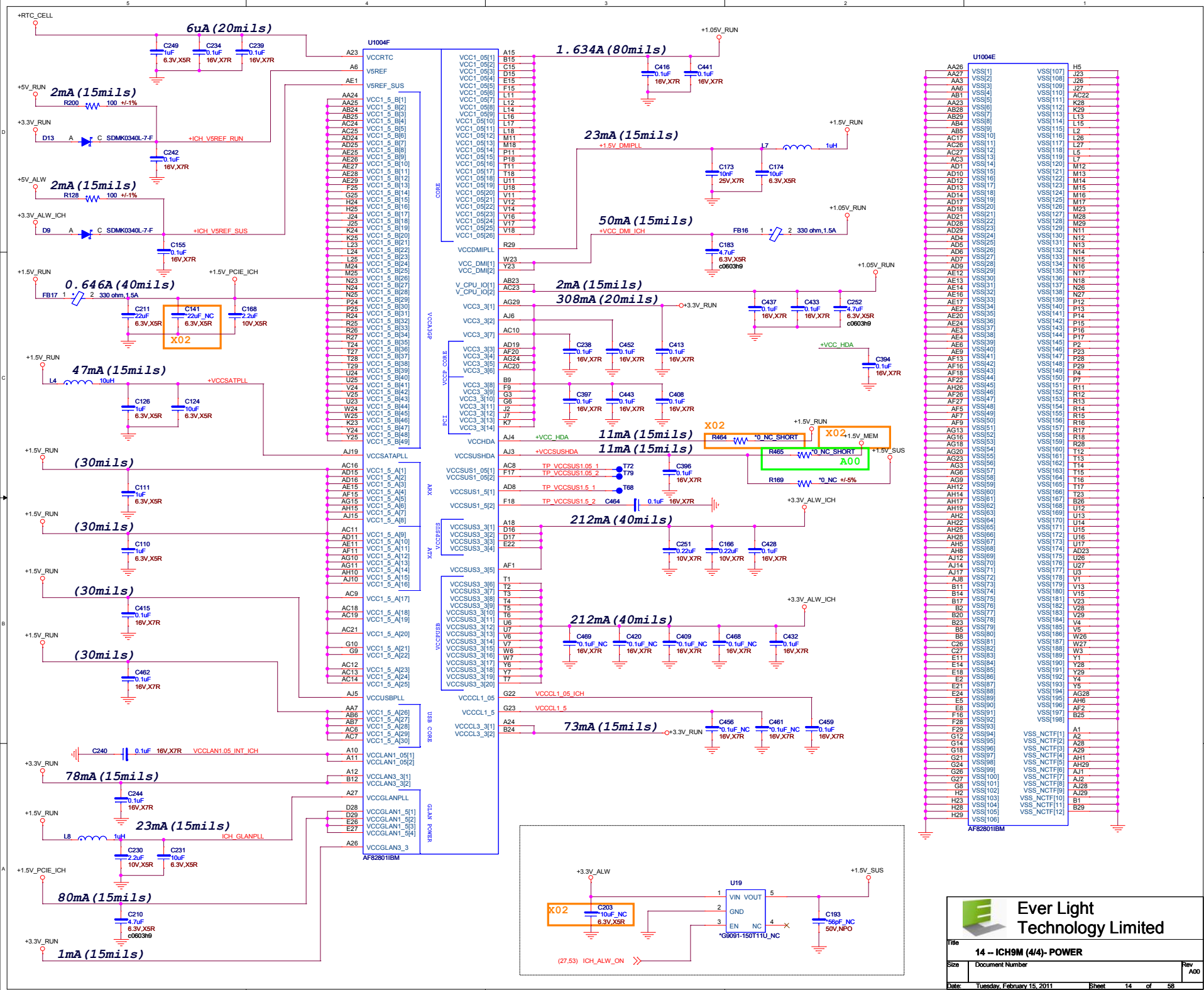
DMI Termination Voltage	
	0 = for desktop applications
GPIO49	1 = for mobile applications Internal PU



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Title		
13 -- ICH9M (3/4)- GPIO		
Size	Document Number	Rev
		A0
Date:	Tuesday, February 15, 2011	Sheet 13 of 58

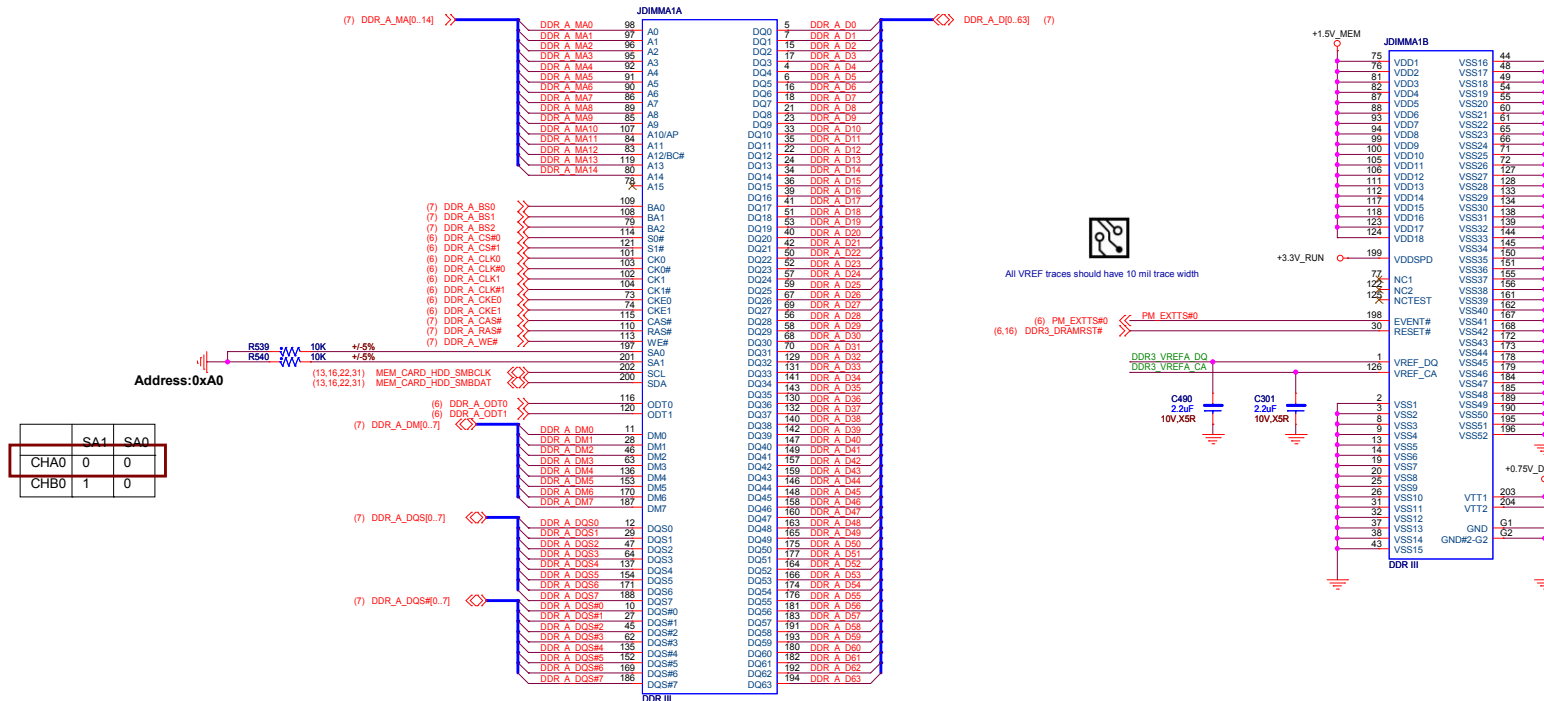




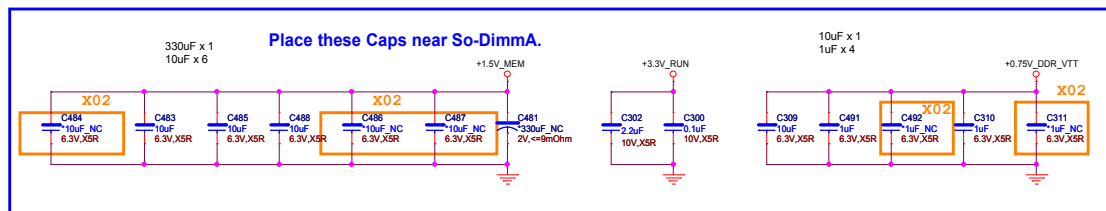


DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

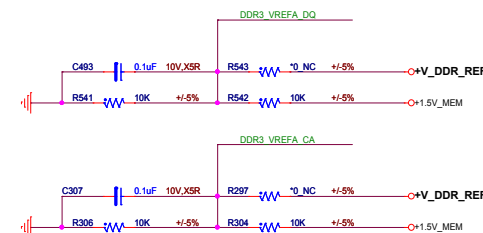
Change to STD type



+1.5V\_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals  
These capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

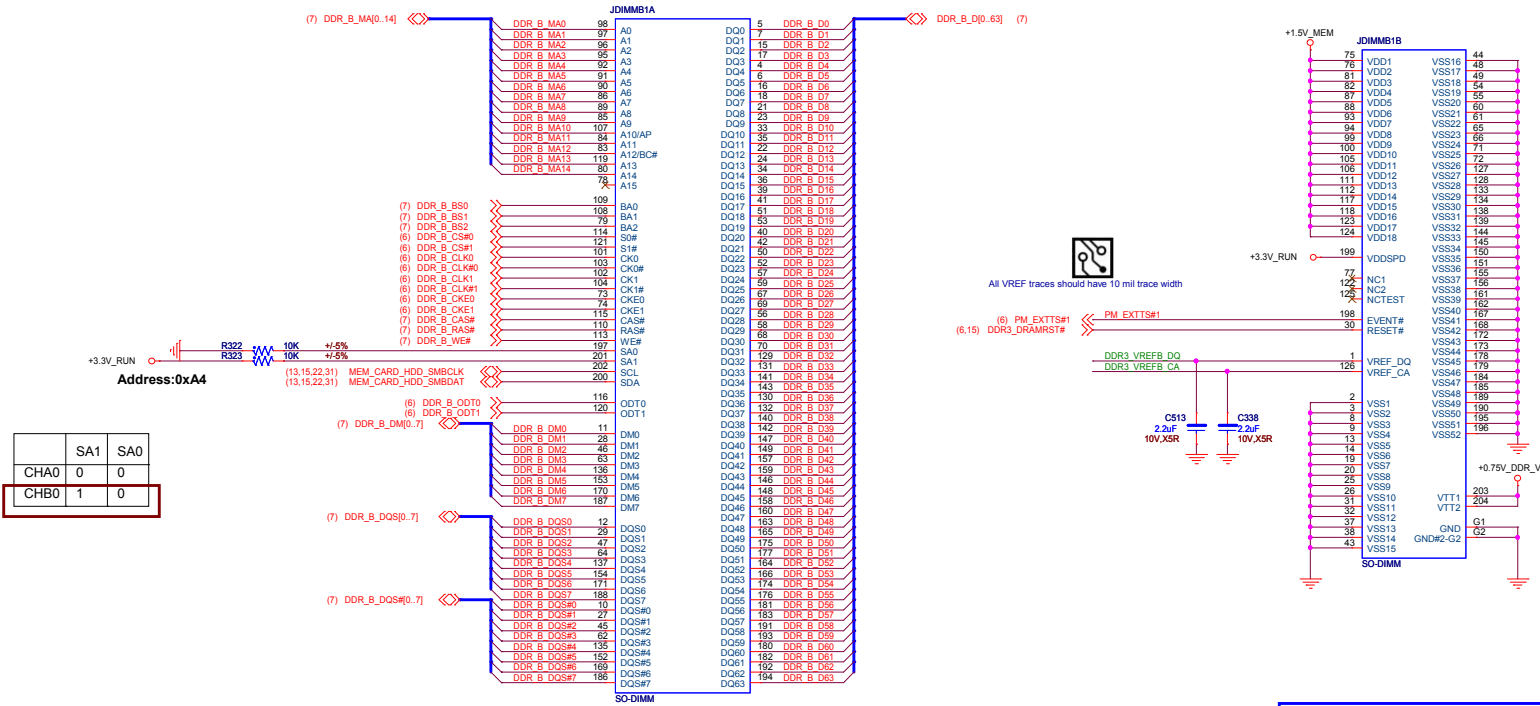


For SO-DIMMA VREF\_DQ /CA

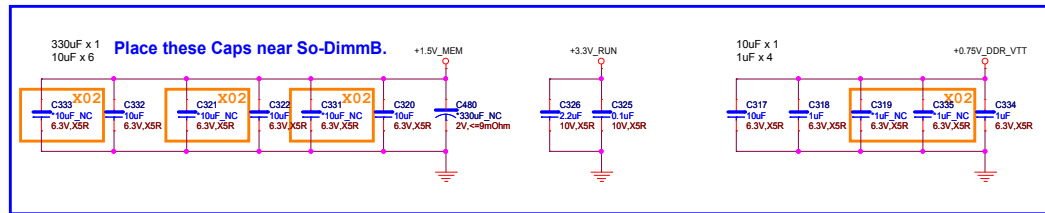


Change to STD type

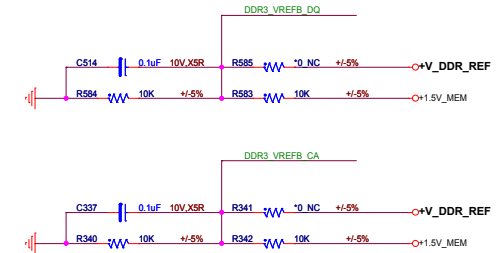
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



+1.5V\_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals. Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector.

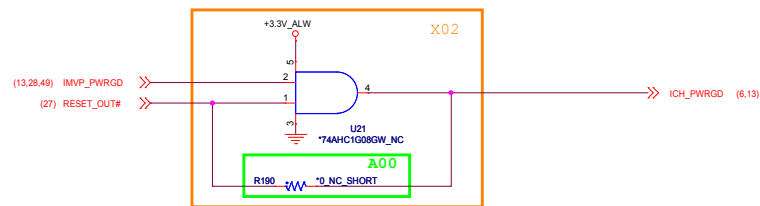
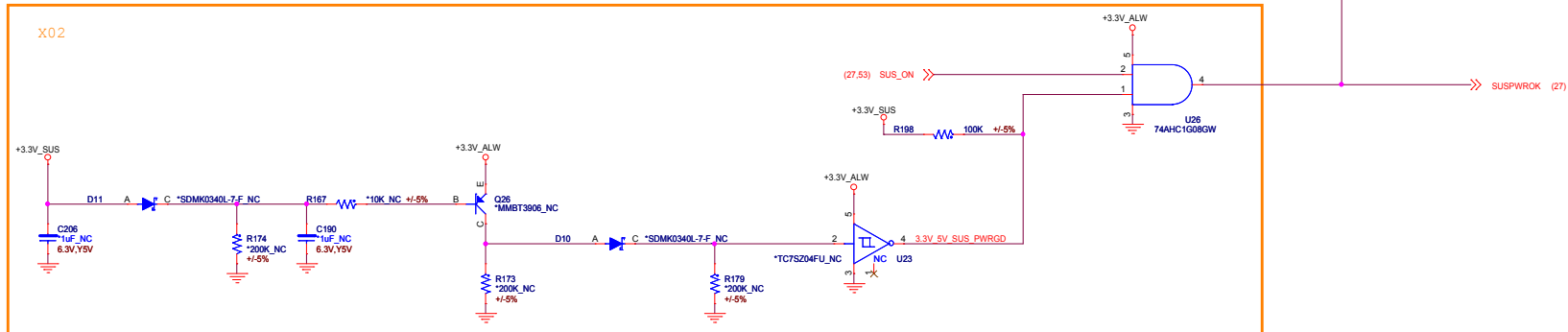
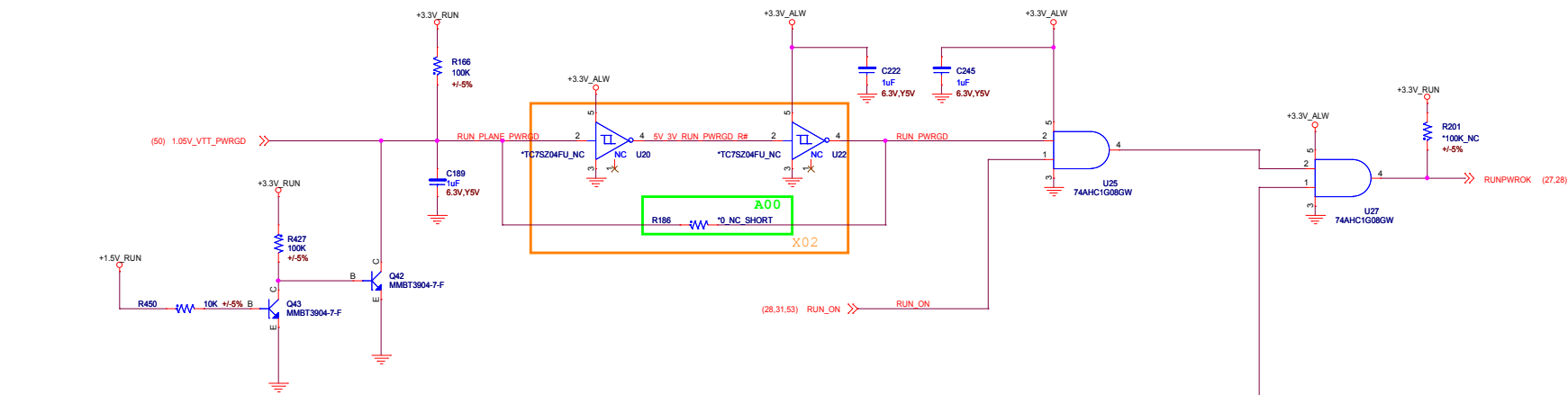


For SO-DIMMB VREF\_DQ /CA



**Ever Light Technology Limited**

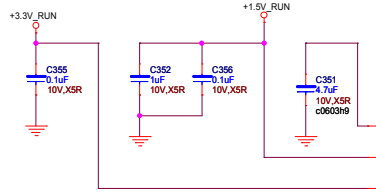
Title		
16 -- SODIMM-204P-B0		
Size	Document Number	Rev
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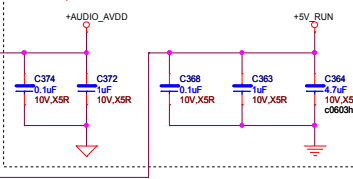


Layout Note:  
Place caps close to codec.

With HDMI DVDD\_IO is  
+1.5V\_RUN



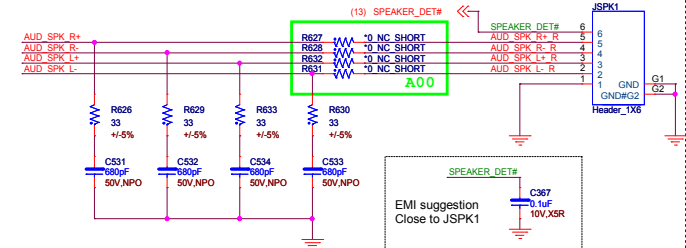
Layout Note:  
Place caps close to codec.



JACK Detect Port Mapping  
SENSE\_A : Port A (39.2K)  
Port B (20K)  
Port C (10K)  
SPDIF0 (5.1K)  
  
SENSE\_B : Port E (39.2K)  
Port F (20K)  
DMIC0 (10K)  
SPDIF1 (5.1K)

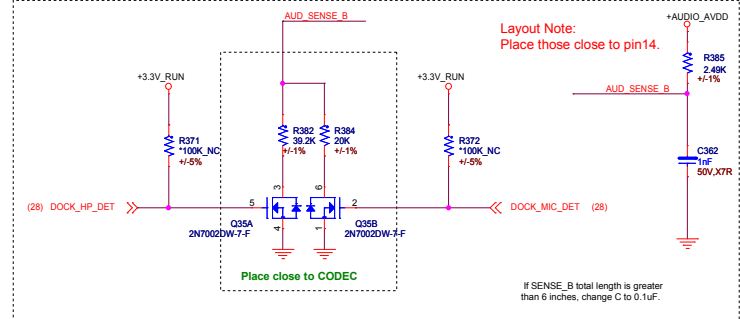
Using 2.49K Pull-up to AVDD

## Speaker Connector

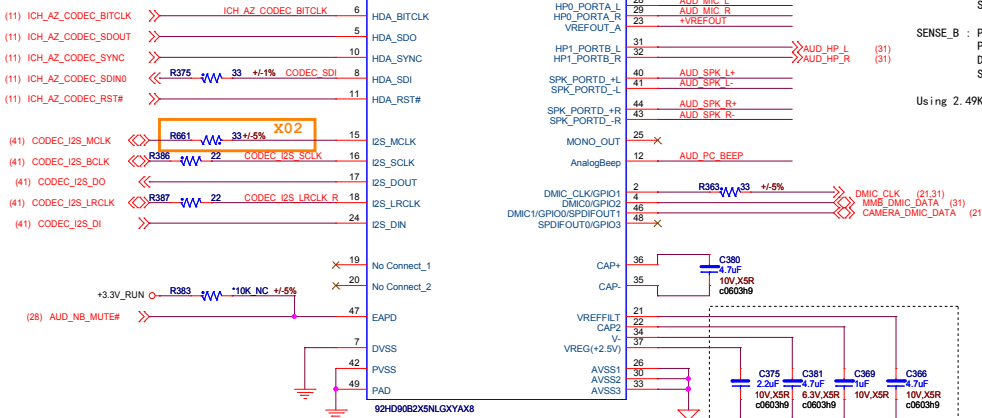


Keep those trace as widely as possible  
that will help to decrease the Power Loss

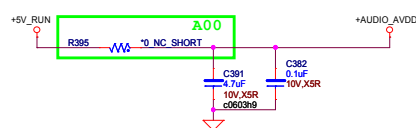
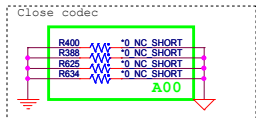
Layout Note:  
Place those close to pin14.



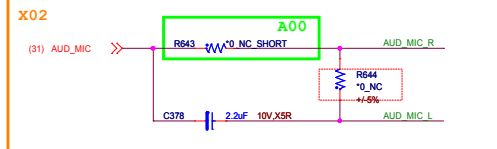
If SENSE\_B total length is greater  
than 6 inches, change C to 0.1uF.



Close codec



X02

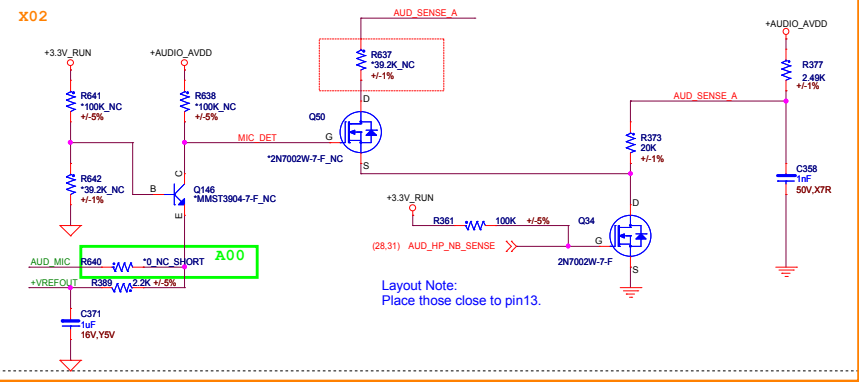


Co Lay Note

Default:uninstall R644,R637  
Install R643

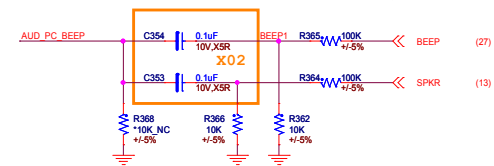
Second:uninstall R643  
Install R644,R637

X02



## PC BEEP

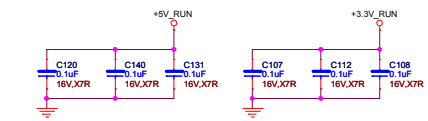
If SENSE\_A total length is greater  
than 6 inches, change C to 0.1uF.



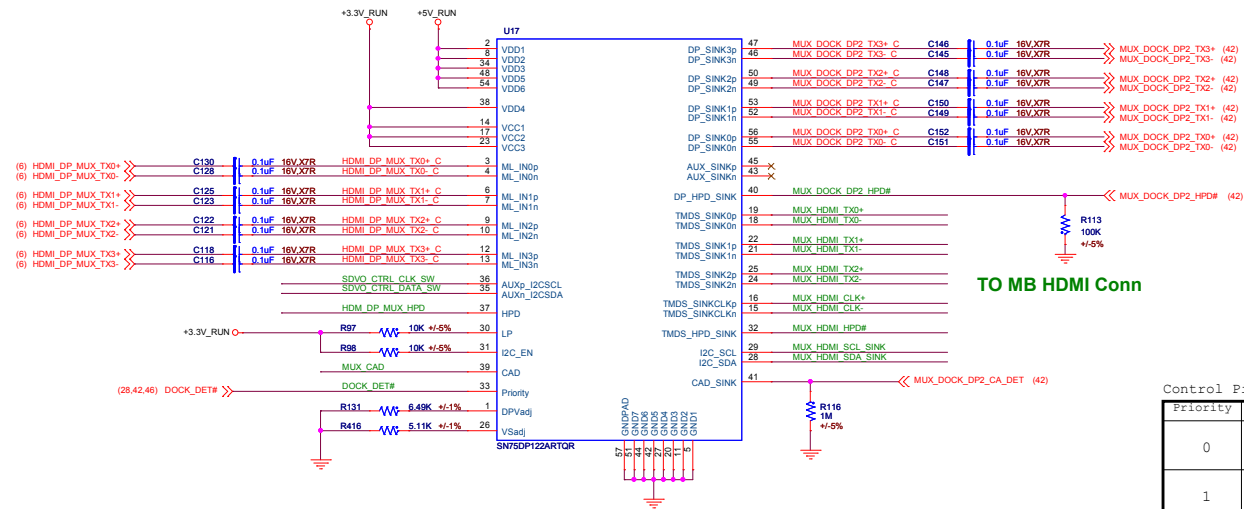
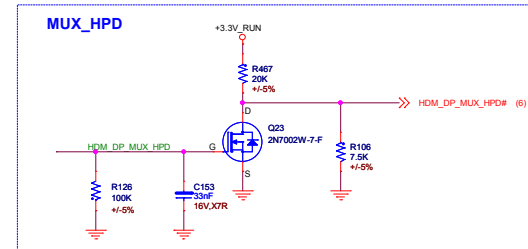
Ever Light  
Technology Limited

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## HDMI & DP MUX



From MCH

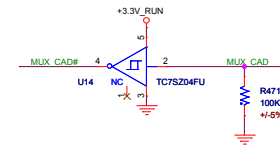
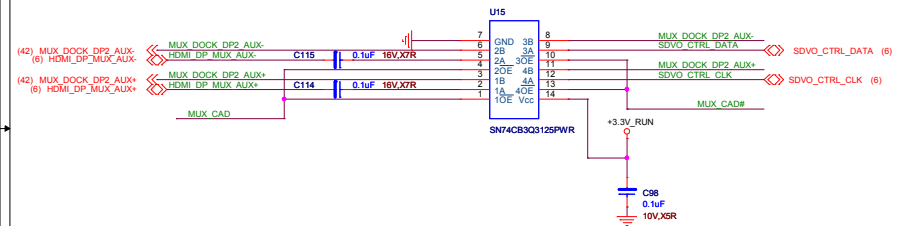


### To Docking DP Port

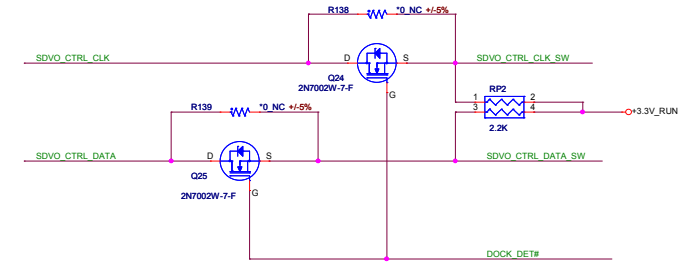
TO MB HDMI Conn

Priority	CAD	STATUS	DESCRIPTION
0	0	DP	If both DP_HPD_SINK and TMDS_HPD_SINK are high, the DP port is selected
1	1	HDMI	If both DP_HPD_SINK and TMDS_HPD_SINK are high, the TMDS port is selected

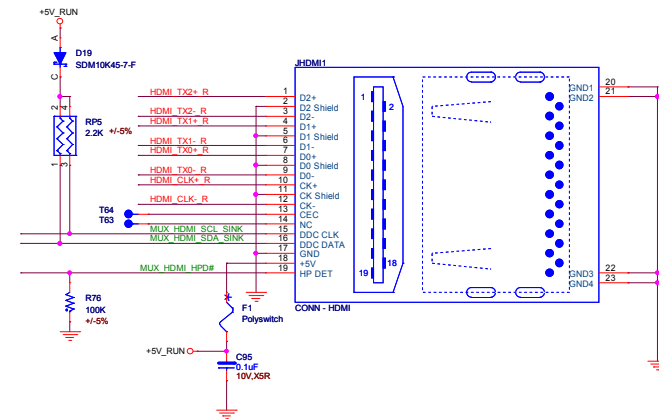
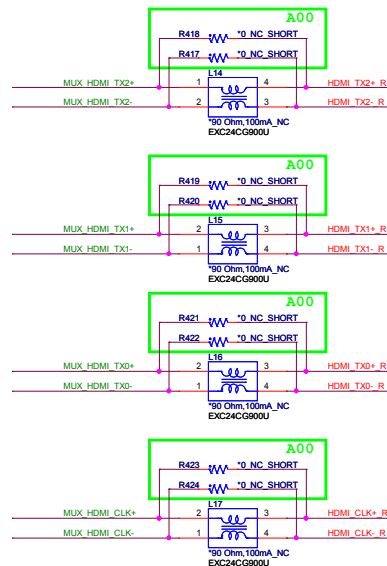
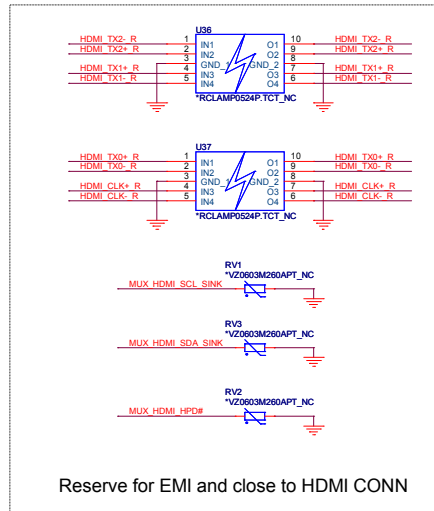
## AUX/DDC SW



## HDMI DDC

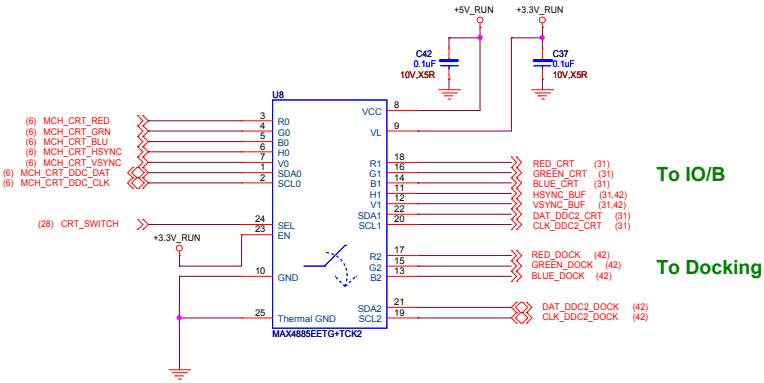


## HDMI CONN



CRT Switch

From MCH



To IO/B

To Docking

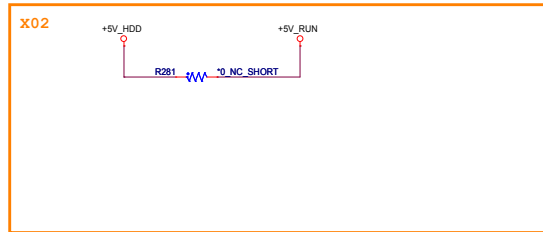
CRT Switch table

SEL	VGA signals	Switch
L	RGB[0] = RGB[1] SDA[0] = SDA[1] SCL[0] = SCL[1]	IOR/B
H	RGB[0] = RGB[2] SDA[0] = SDA[2] SCL[0] = SCL[2]	DOCK

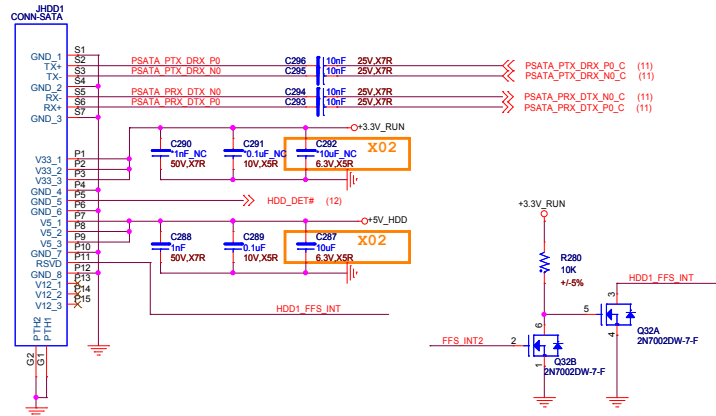




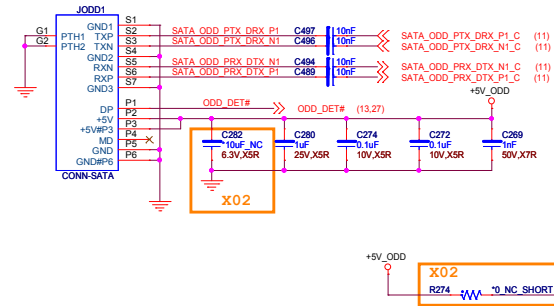
## HDD POWER



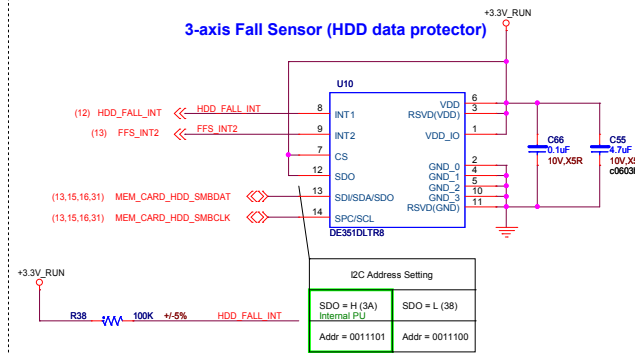
### HDD Connector



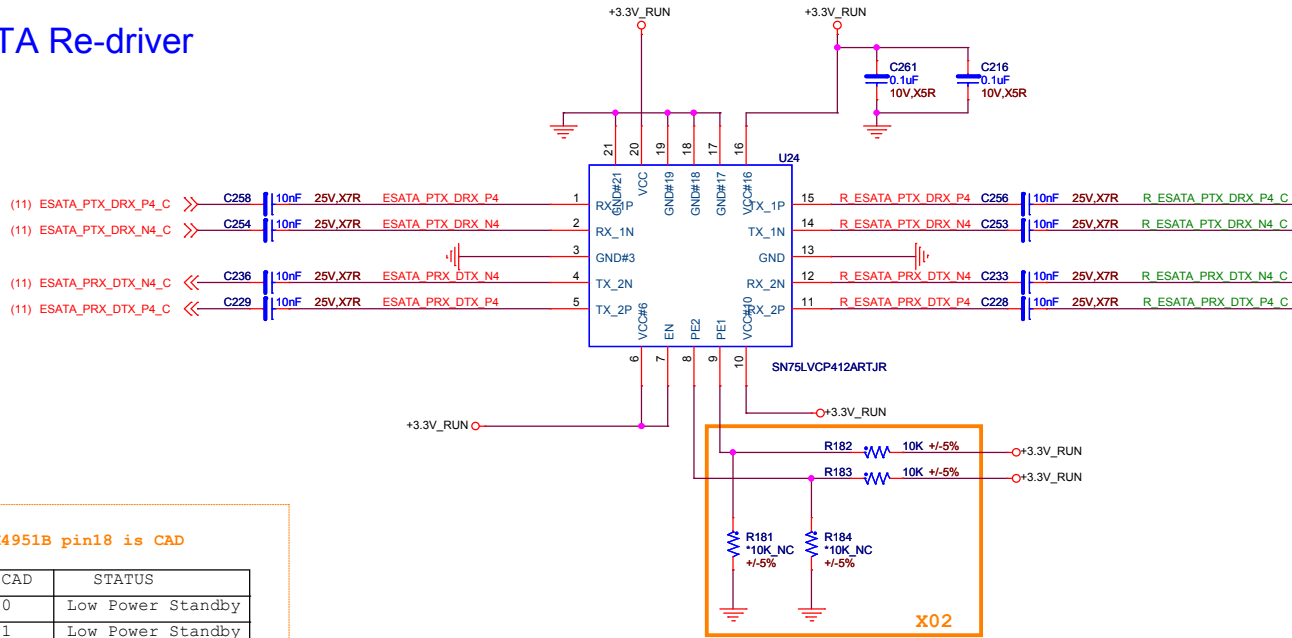
### ODD Connector



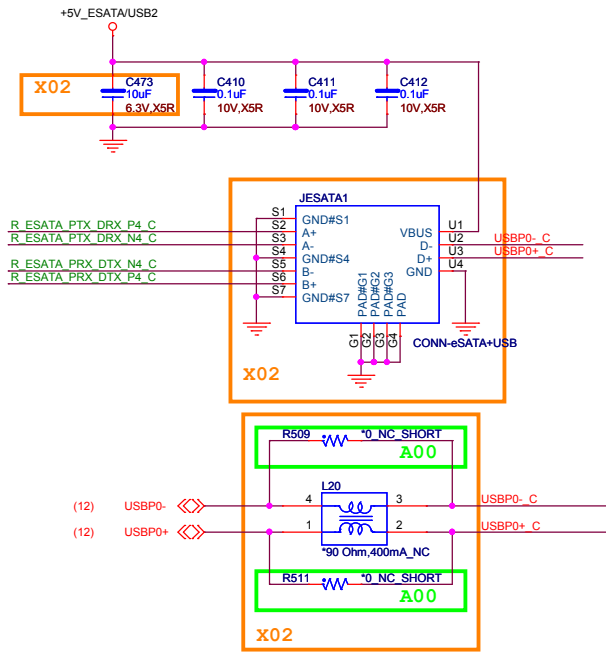
### 3-axis Fall Sensor (HDD data protector)



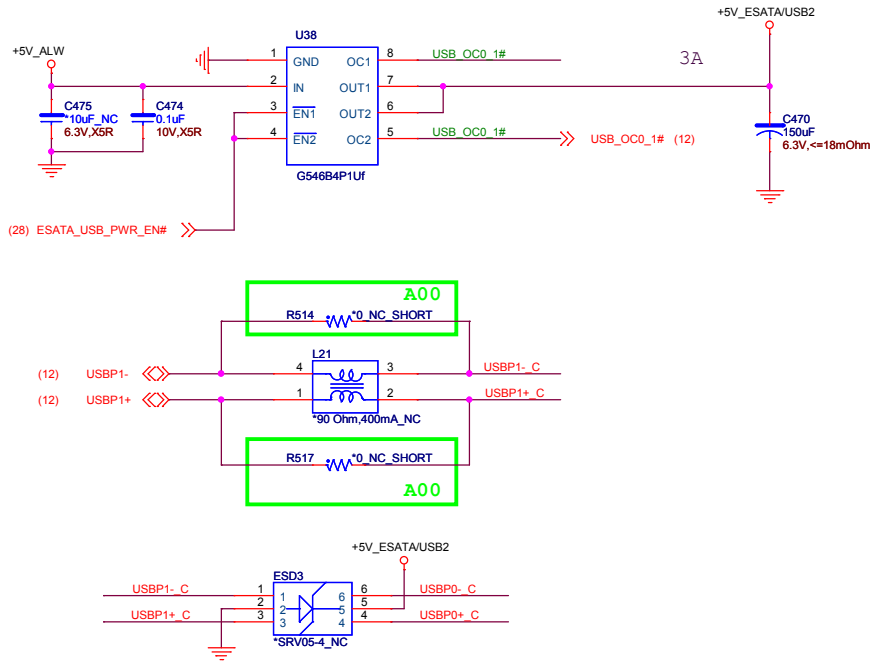
ESATA Re-driver



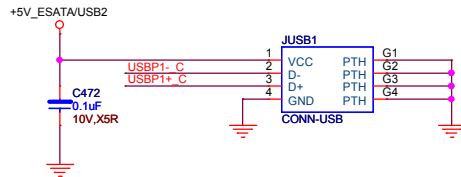
USB+eSATA

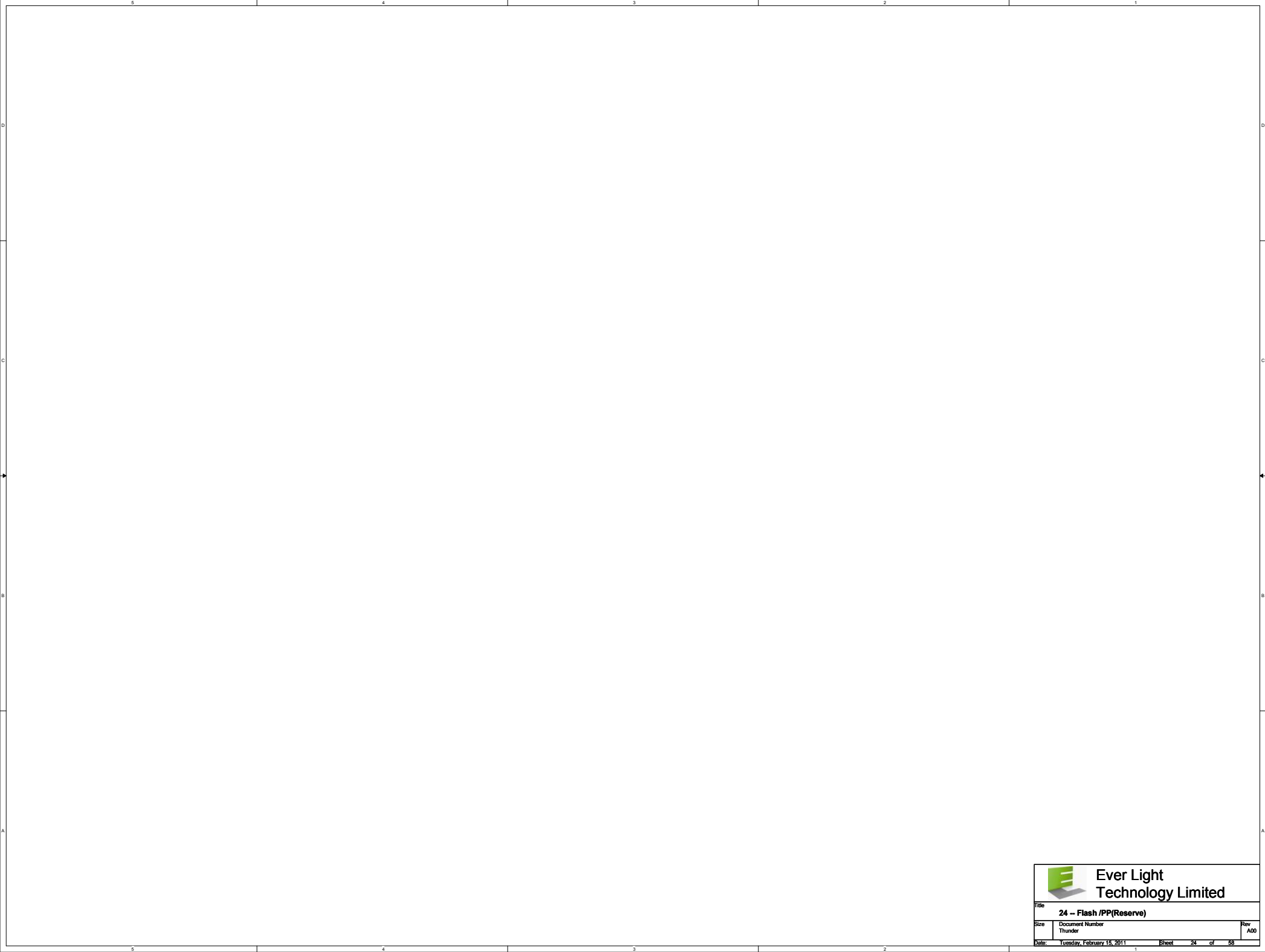



USB Power



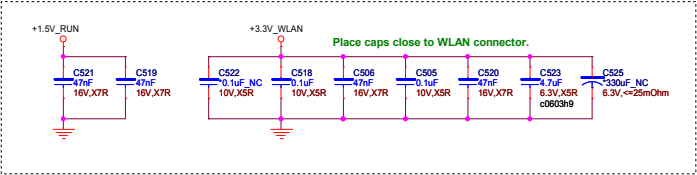
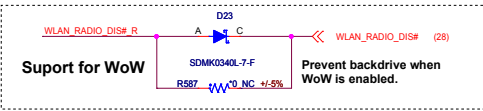
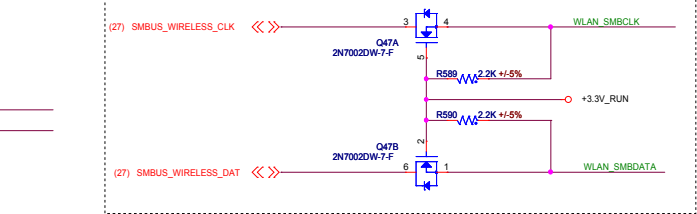
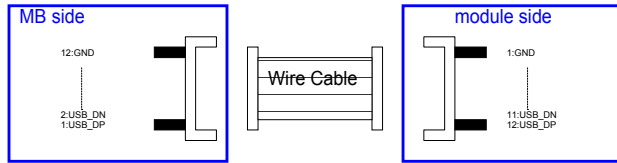
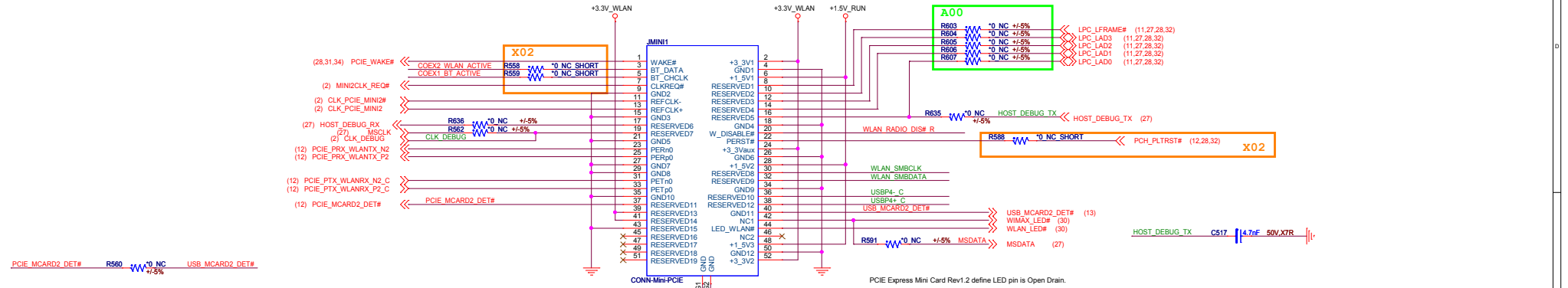
USB(Back Side)



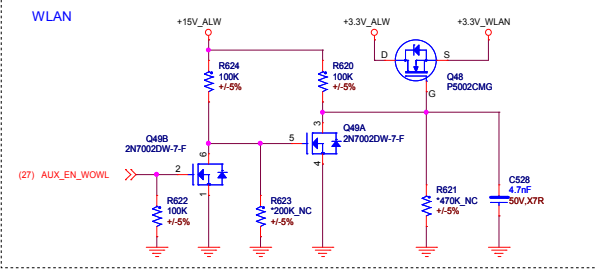
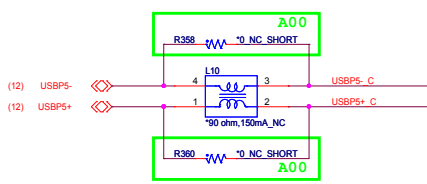
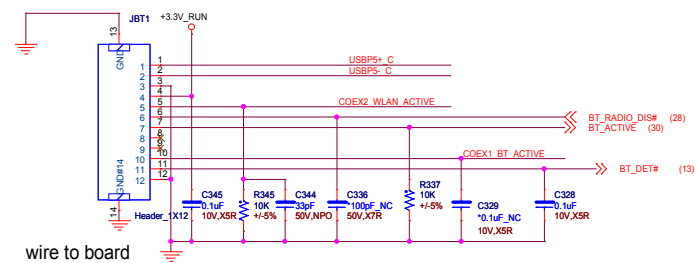


			<b>Ever Light Technology Limited</b>		
<b>Title</b> 24 -- Flash /PP(Reserve)					
<b>Size</b>	<b>Document Number</b>				<b>Rev</b>
	Thunder				A00
<b>Date:</b> Tuesday, February 15, 2011					
<b>Sheet</b> 24 <b>of</b> 58					

# MiniCard WLAN connector (WLAN, half size)



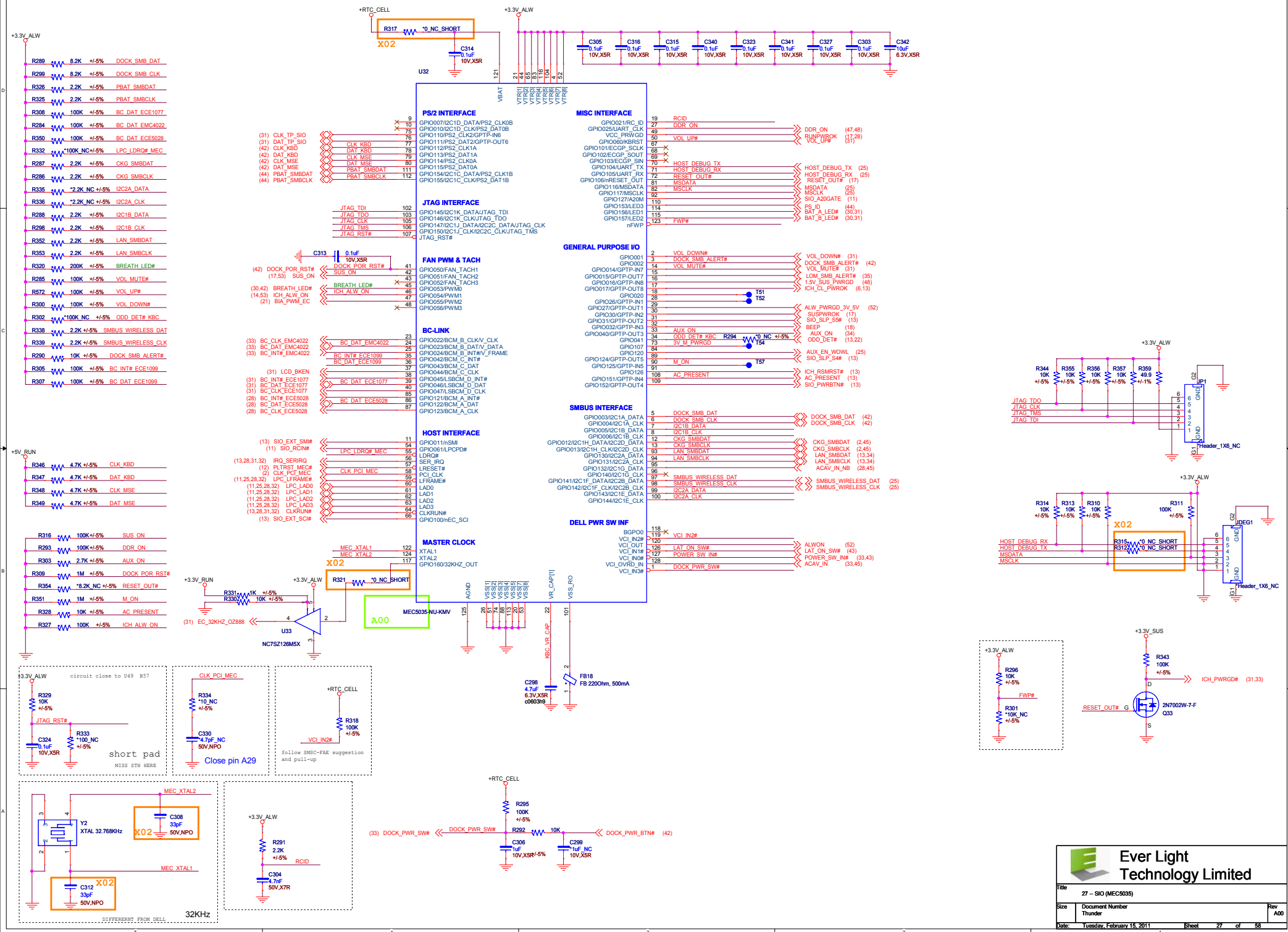
## Bluetooth Support Blamey stone 375



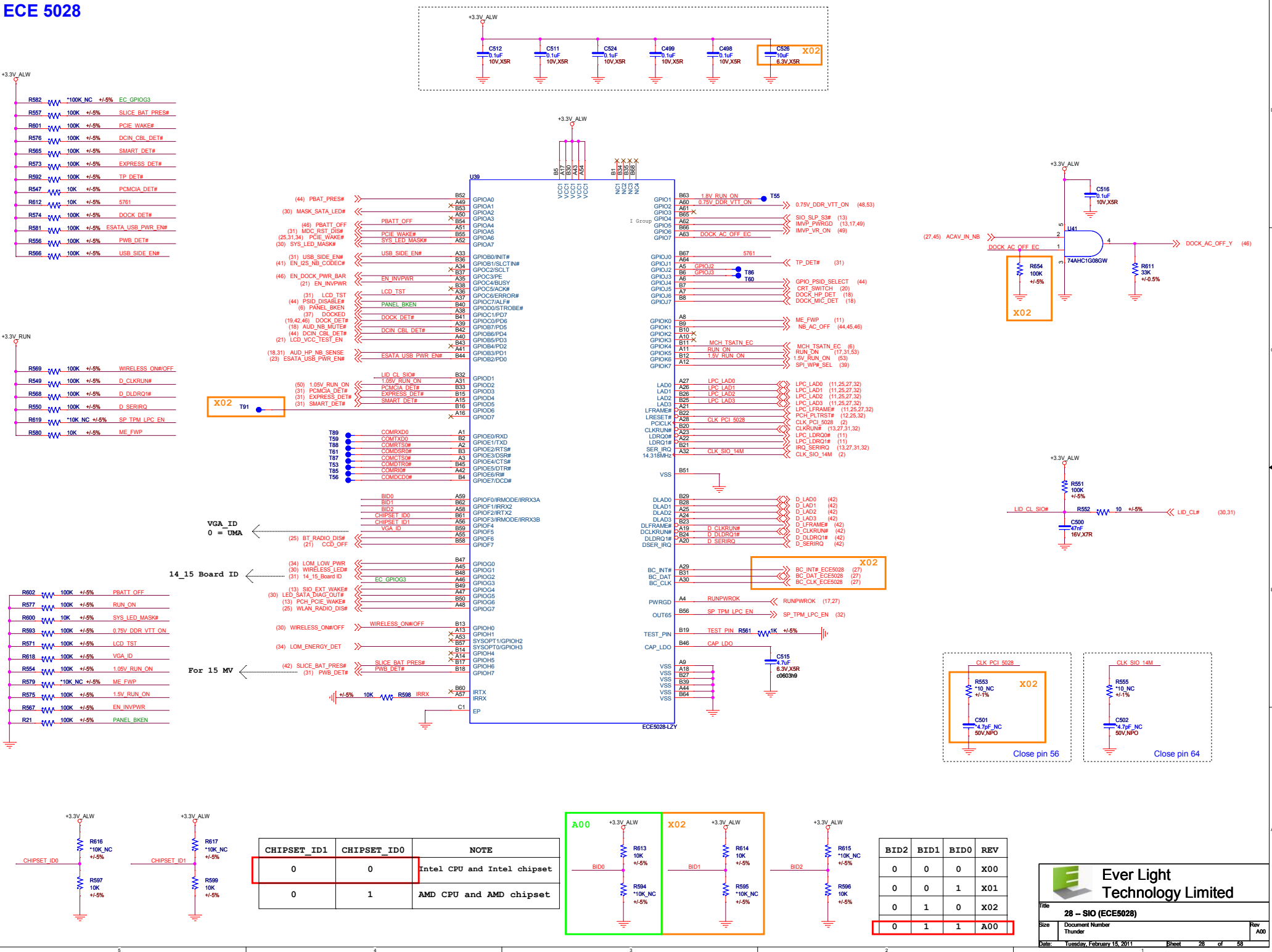




# MEC 5035

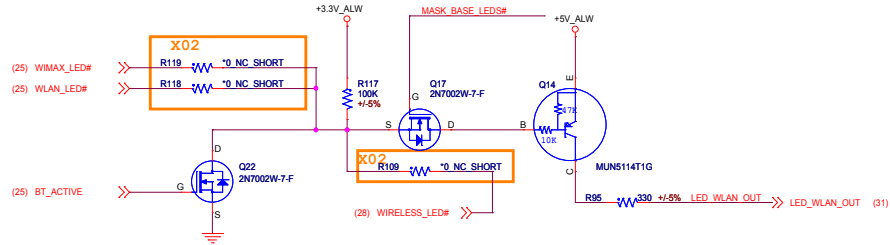


# ECE 5028





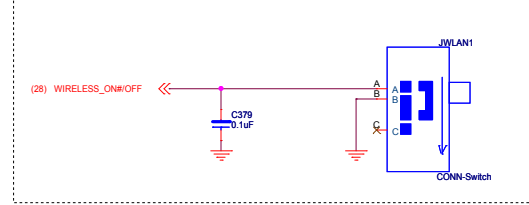
## WLAN



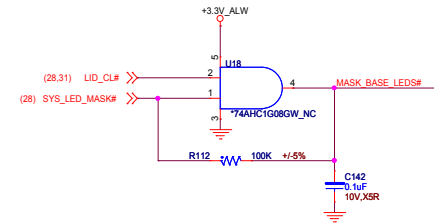
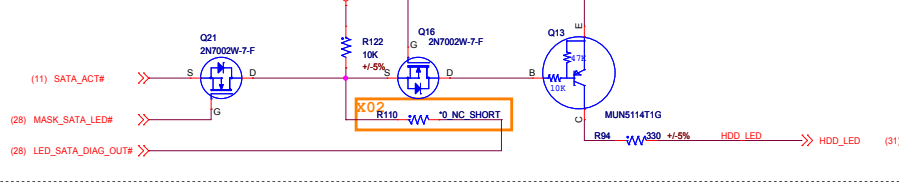
From TOP View:



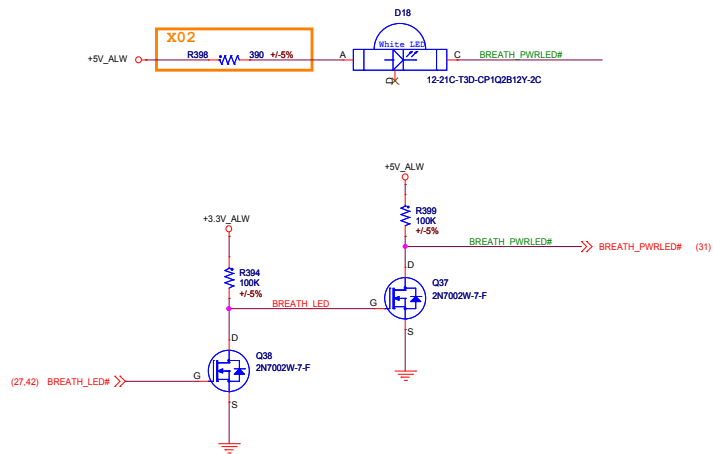
## Wireless SW



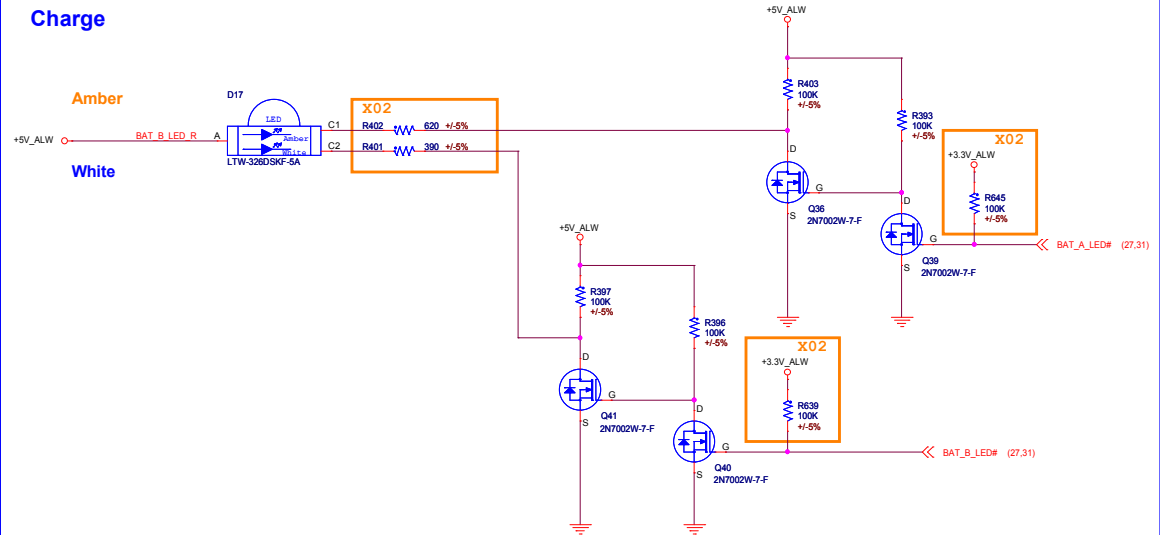
## HDD



## BREATH PWRLD

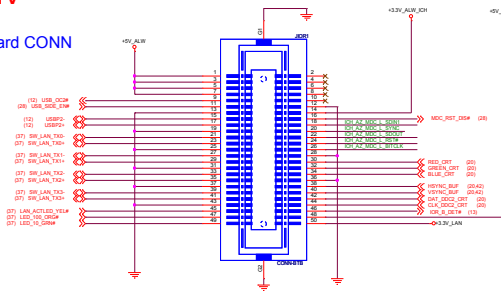


## Charge

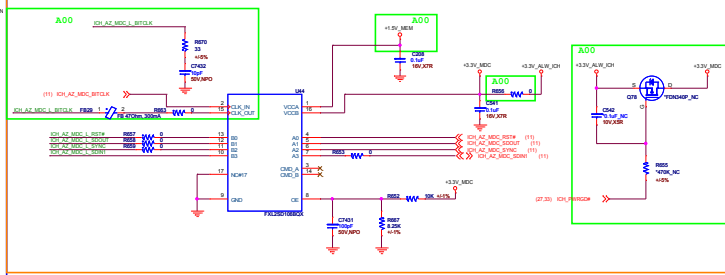


# 14 MV

## I/O Board CONN



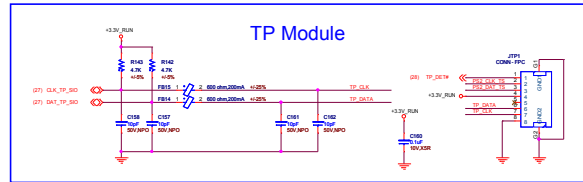
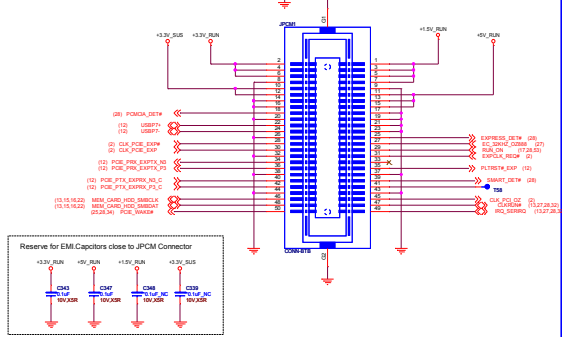
## MDC Level Shift X02



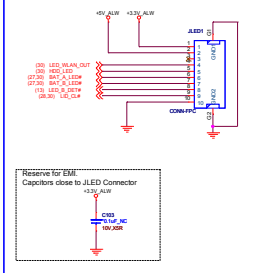
## TPM Board CONN X02



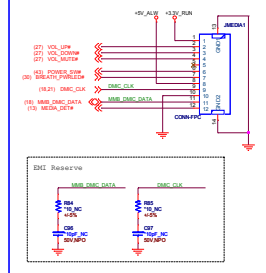
## Express Card Board CONN



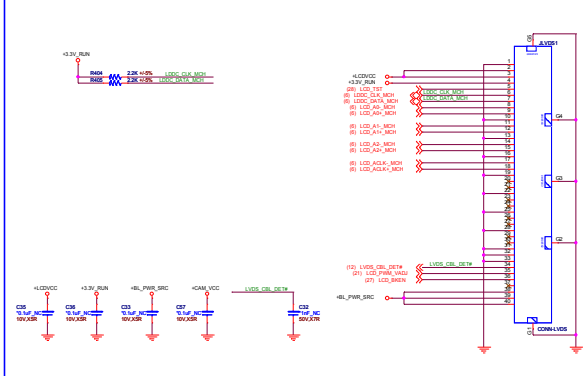
## LED Board CONN



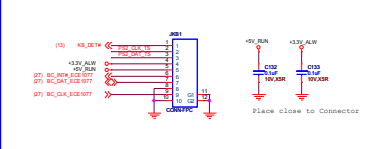
## Media Board CONN



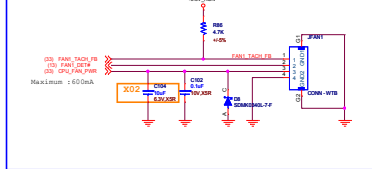
## LVDS CONN



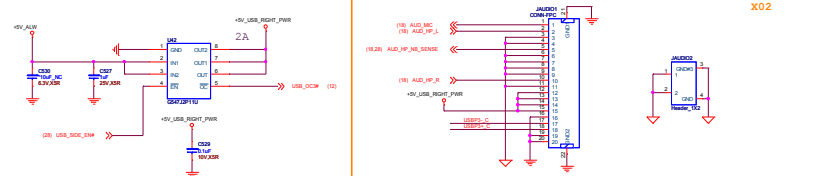
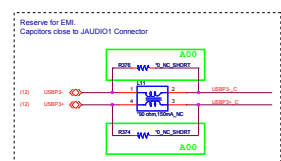
## Keyboard Module



## CPU Fan



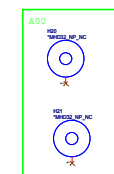
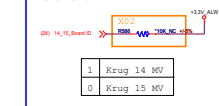
## Audio Board CONN



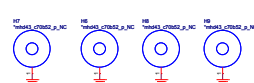
## PowerB DET



## 14&15 Board ID



## For CPU Heatsink



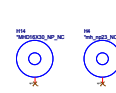
## New Card NUT



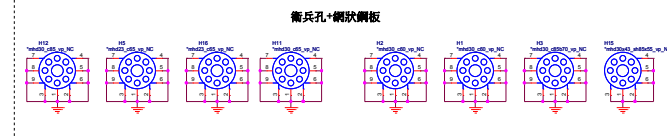
## DB NUT



## GMCH NUT



## 備兵孔・網狀銅板

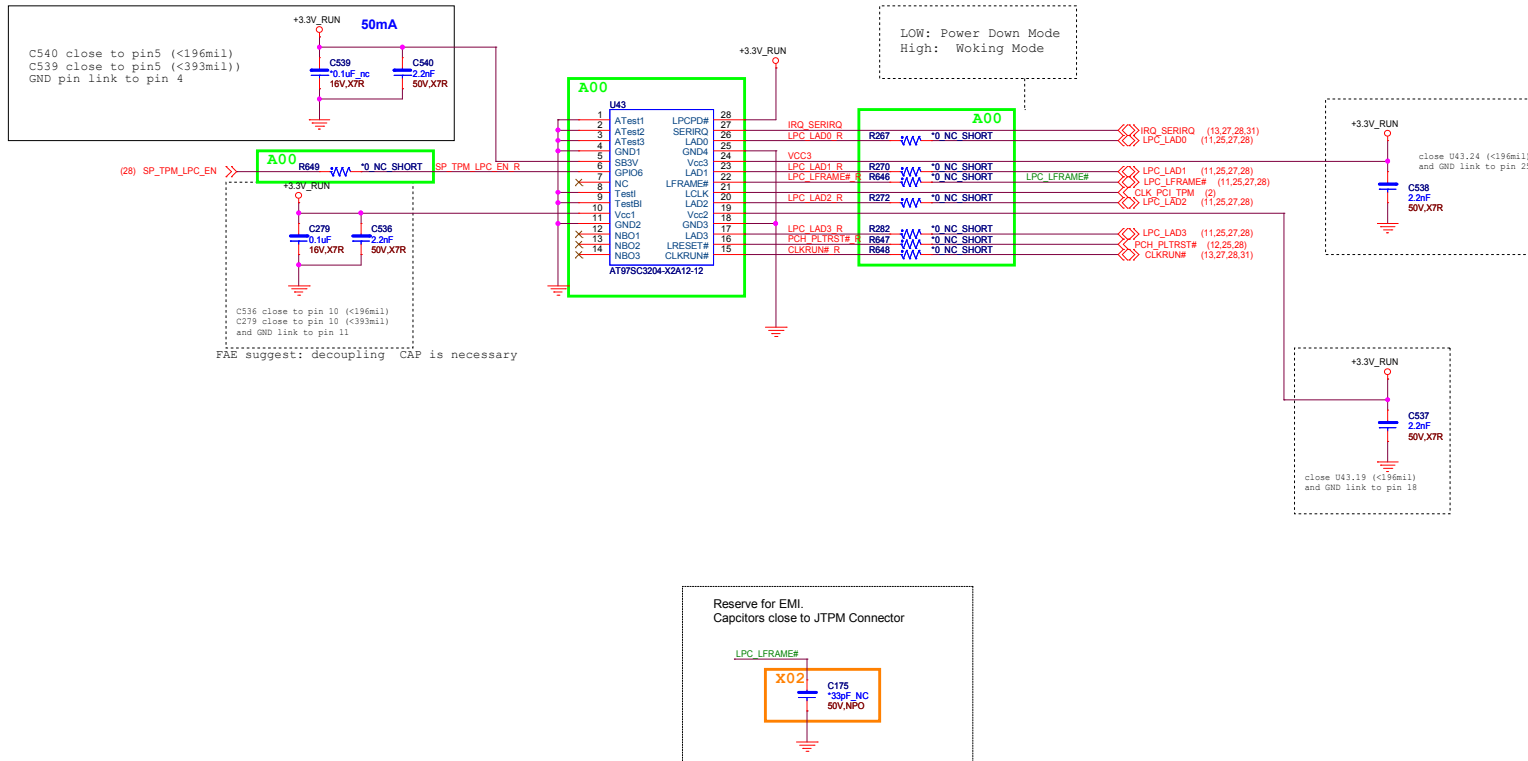


## X02



x02

## China TPM : ATMEL

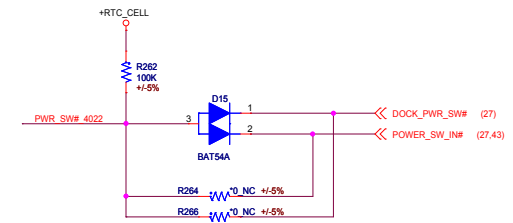
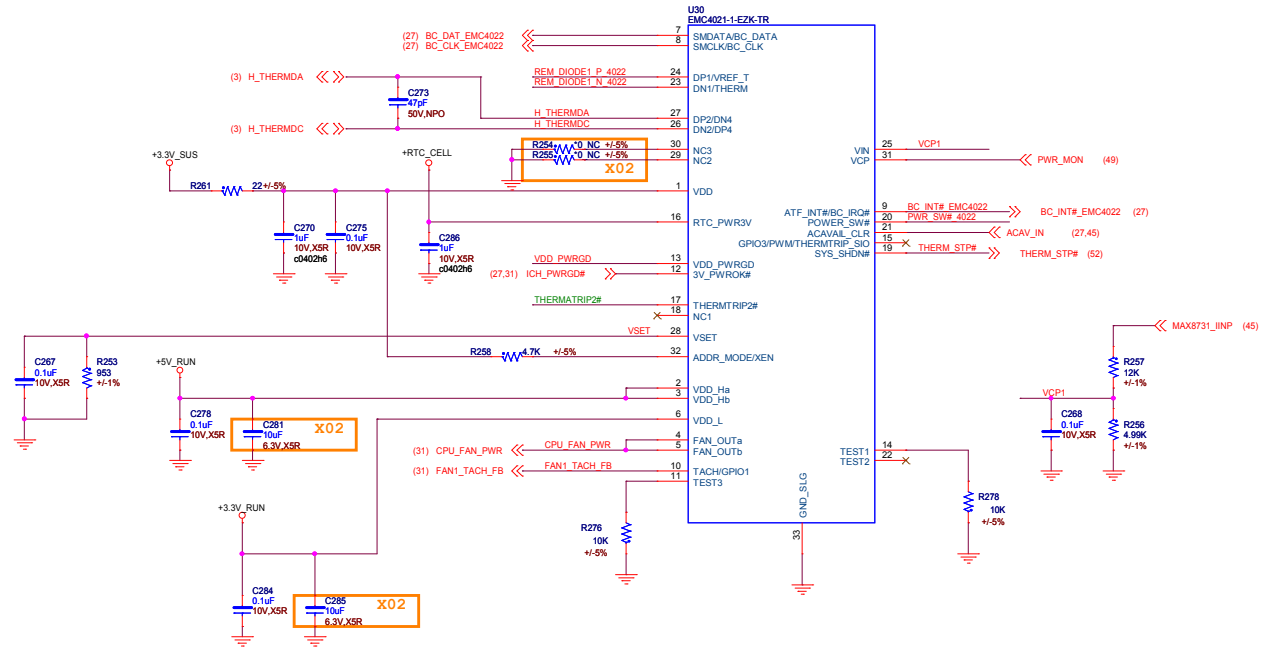
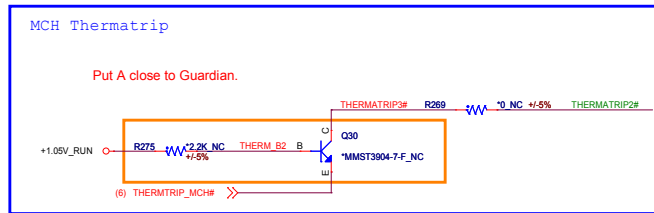
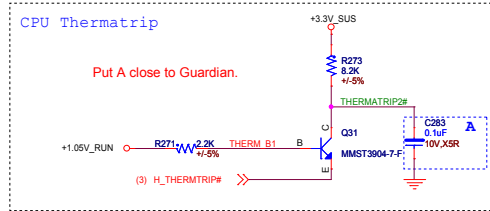
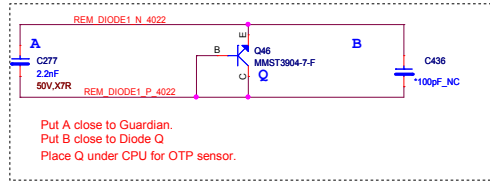




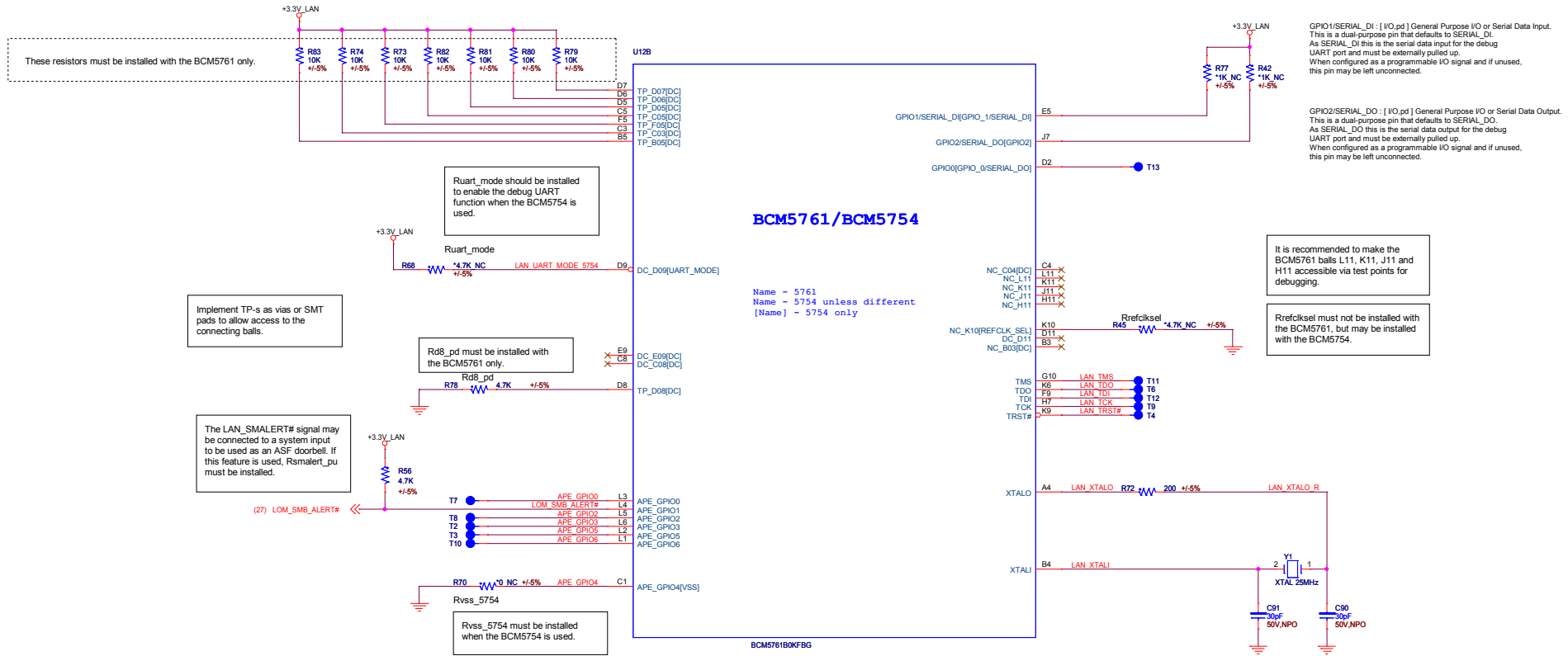
# EMC4022, EMC4021 co-layer Note

EMC4022: uninstall R878, R879, R880  
Install R849, C808

EMC4021: uninstall R849, C808  
Install R878, R879, R880







GPIO1/SERIAL\_DI : [ I/O.pd ] General Purpose I/O or Serial Data Input.  
This is a dual-purpose pin that defaults to SERIAL\_DI.  
As SERIAL\_DI this is the serial data input for the debug  
UART port and must be externally pulled up.  
When configured as a programmable I/O signal and if unused,  
this pin may be left unconnected.

GPIO2/SERIAL\_DO : [ I/O.pd ] General Purpose I/O or Serial Data Output.  
This is a dual-purpose pin that defaults to SERIAL\_DO.  
As SERIAL\_DO this is the serial data output for the debug  
UART port and must be externally pulled up.  
When configured as a programmable I/O signal and if unused,  
this pin may be left unconnected.

It is recommended to make the  
BCM5761 balls L11, K11, J11 and  
H11 accessible via test points for  
debugging.

Rrefclkse1 must not be installed with  
the BCM5761, but may be installed  
with the BCM5754.



36nH is a suggested value.  
Actual value will be system dependent.  
Must use 0603 package for lower DC resistance.

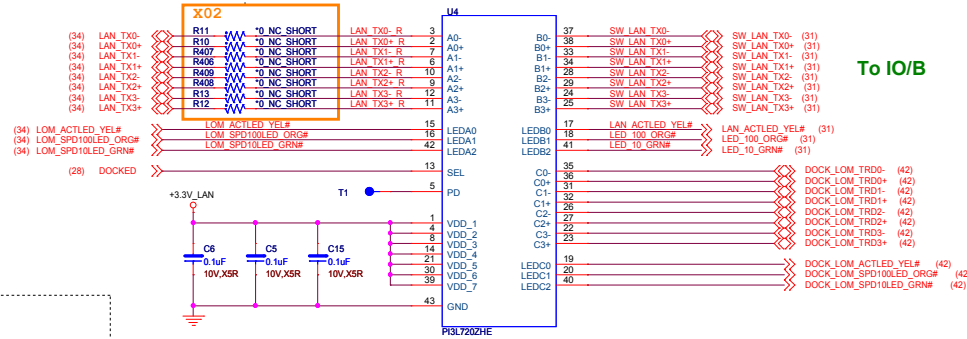
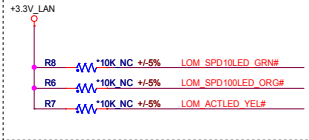
From 5761

To IO/B

To Docking

DOCKED  
SEL 0: RJ45.  
SEL 1: Dock.

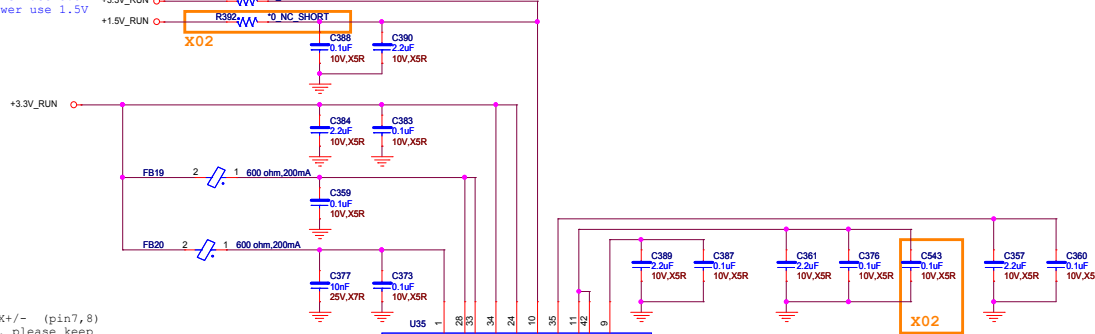
Reserve pull up.



LAN Switch table

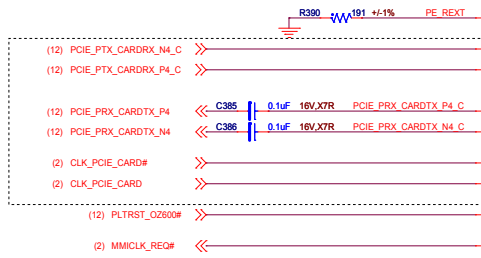
DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LED <sub>Ax</sub> to LED <sub>Bx</sub>	MB
H	Ax to Cx	LED <sub>Ax</sub> to LED <sub>Cx</sub>	DOCK

For REV A, power use 3.3V  
For REV B, power use 1.5V

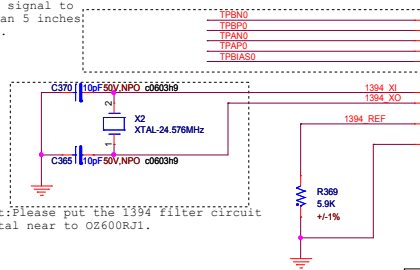


3/25 OZ FAE suggest:PCI-e interface, TX+/- (pin 7,8) and RX+/- (pin 5,6), CLK\_PCIE Card +/- please keep equal length with 100ohm impedance.  
R926,C890 and C891 close to U67

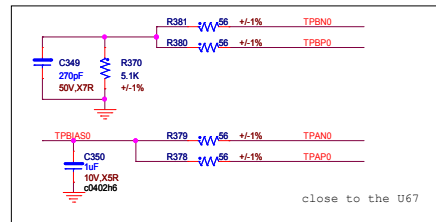
For REV A, R936 use 5.1K  
For REV B, R936 use 191R



3/25 OZ FAE suggest:1394 signal to connector should less than 5 inches, with 90-110ohm impedance.



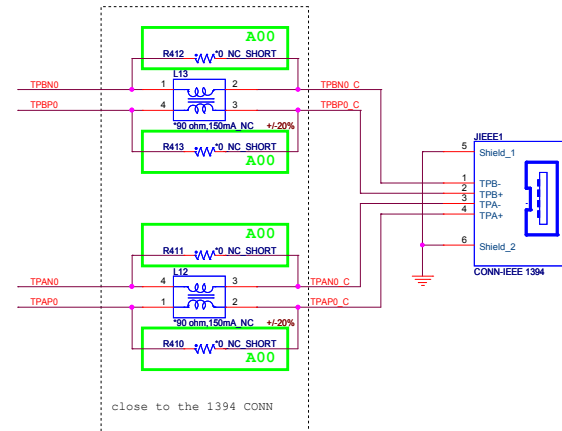
3/25 OZ FAE suggest:Please put the 1394 Filter circuit and 24.576Mhz crystal near to OZ600RJ1.



close to the U67

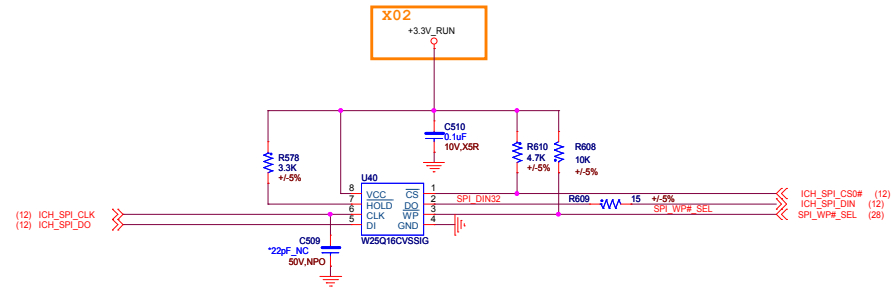
1394a

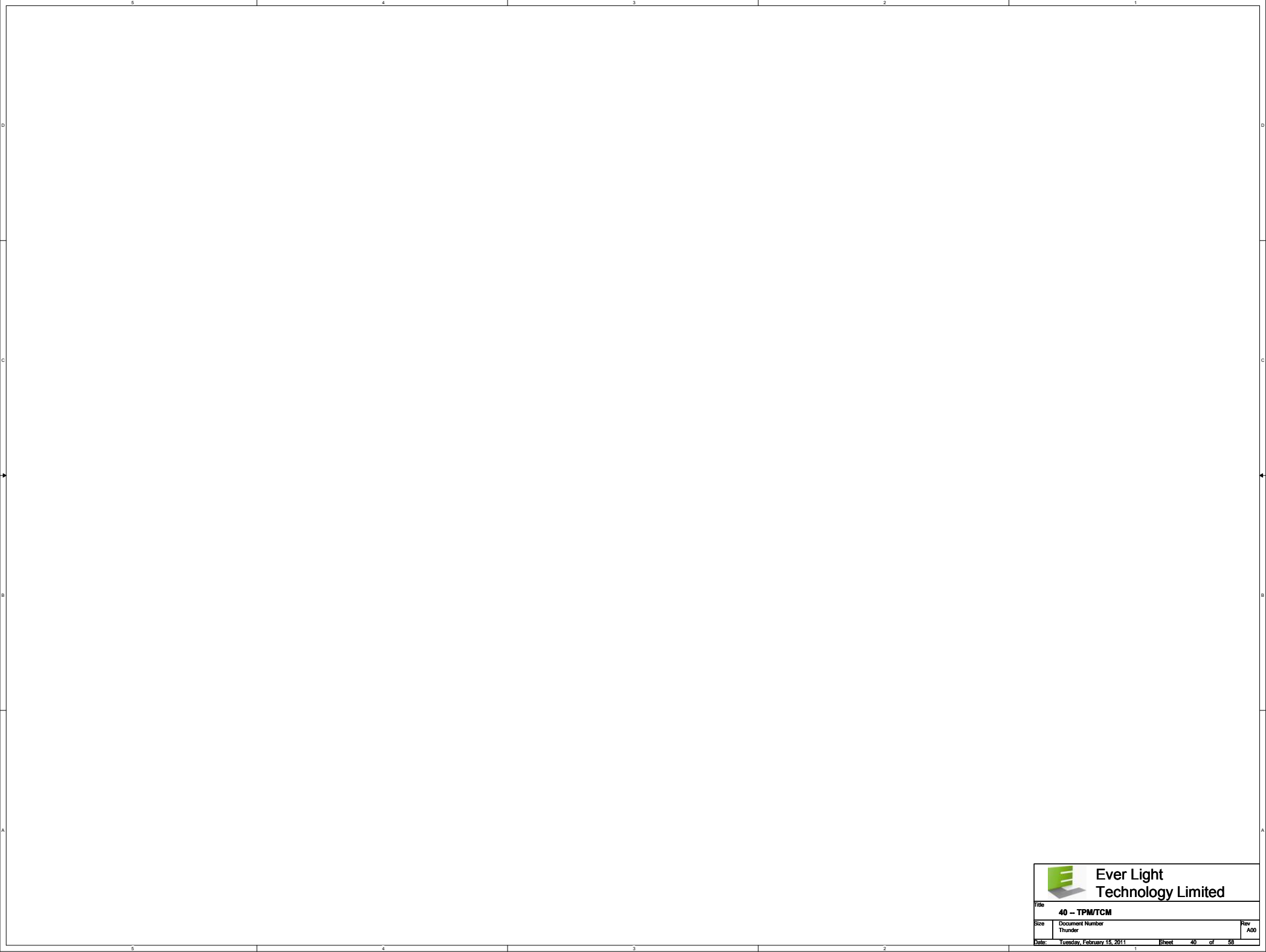
Layout note:  
3/25 OZ FAE suggest:Please care the SD interface layout, it is around 208Mhz clock speed, please control the SD card signals as equal length .




close to the 1394 CONN

# SPI ROM For BIOS (2M Byte)

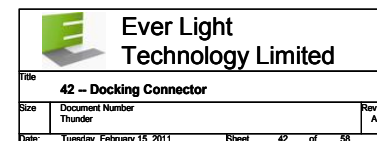


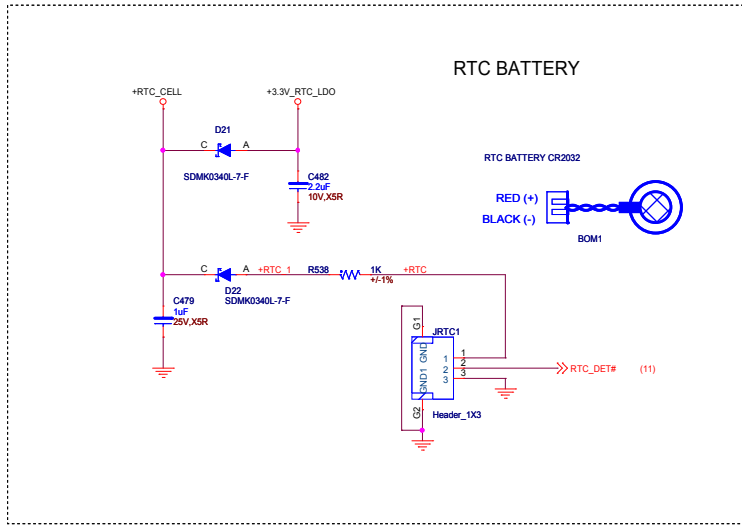


 Ever Light Technology Limited		
Title 40 -- TPM/TCM		
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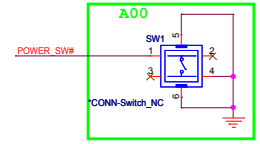
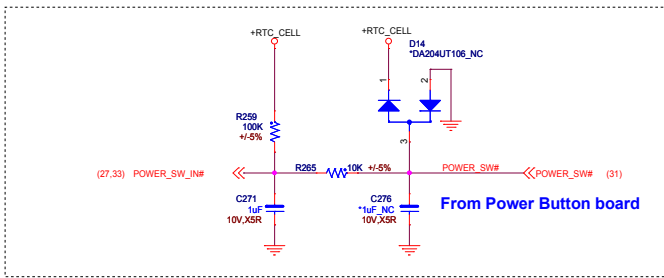
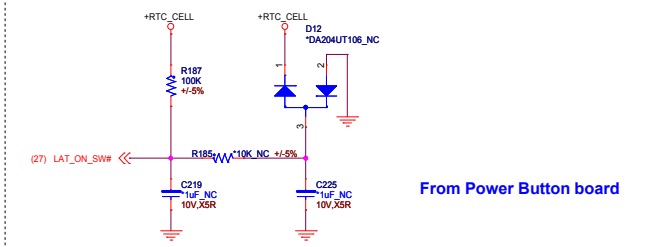




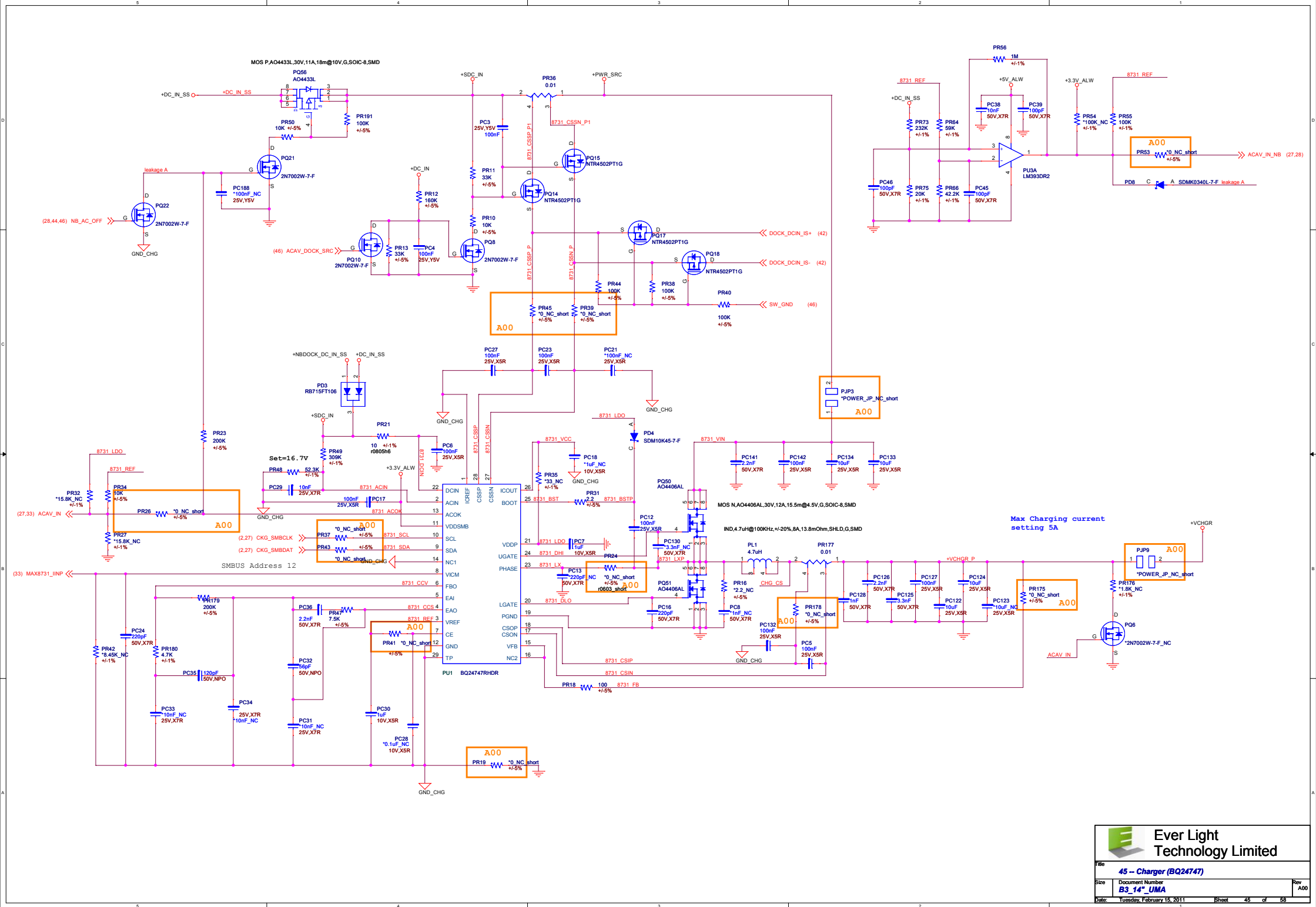




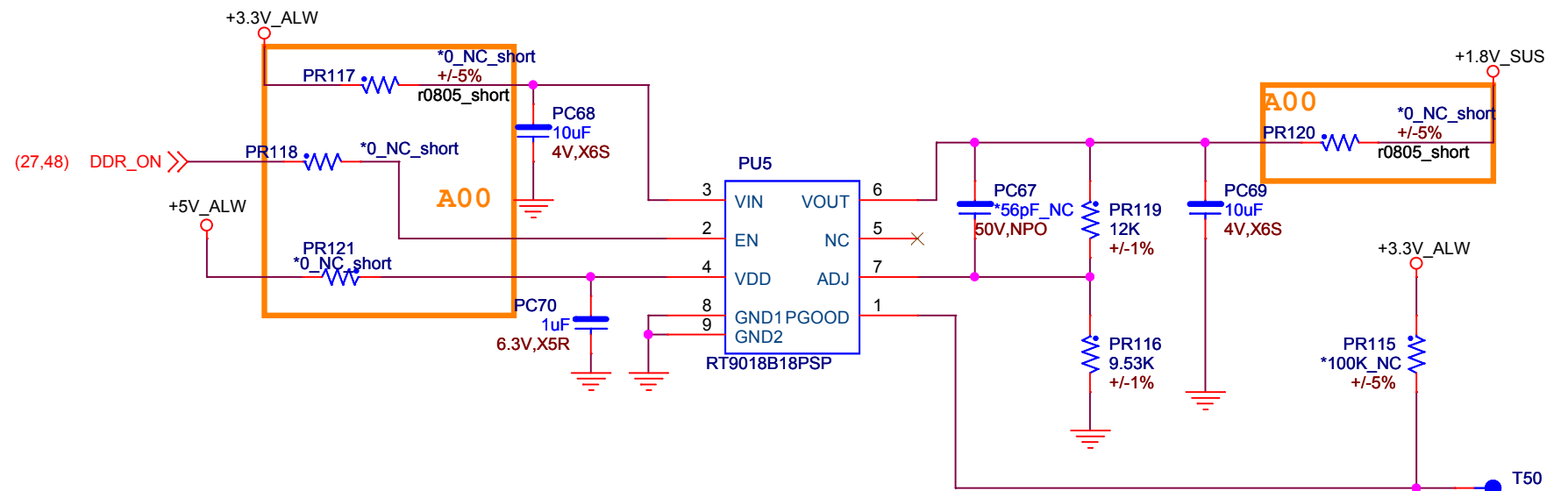
**Precision On (Krug MV is not support)**











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Title

47 -- PW\_SW\_+1.8V(RT9018B)

Size

Document Number

Rev  
A00

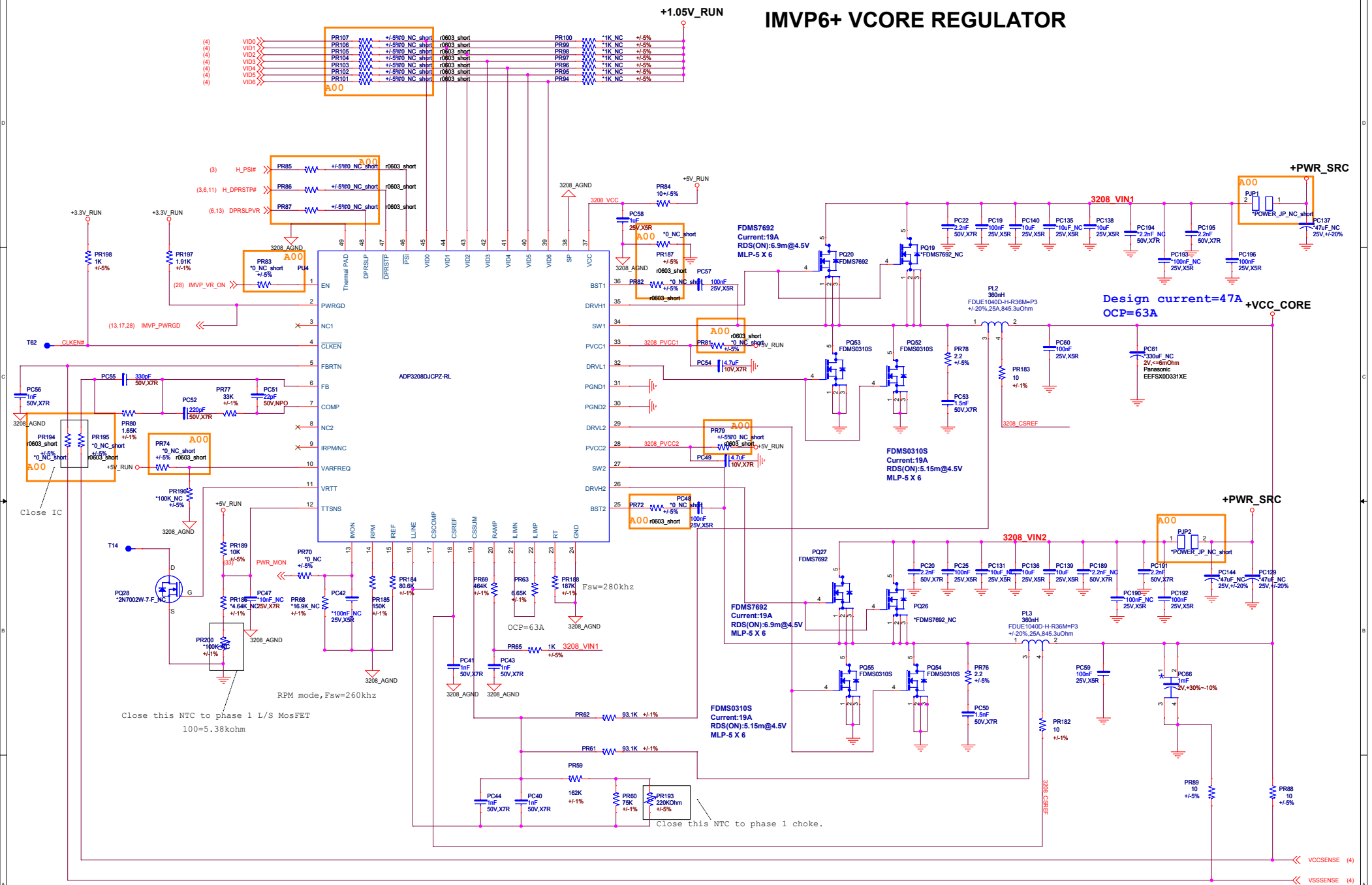
Date: Tuesday, February 15, 2011

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## IMVP6+ VCORE REGULATOR





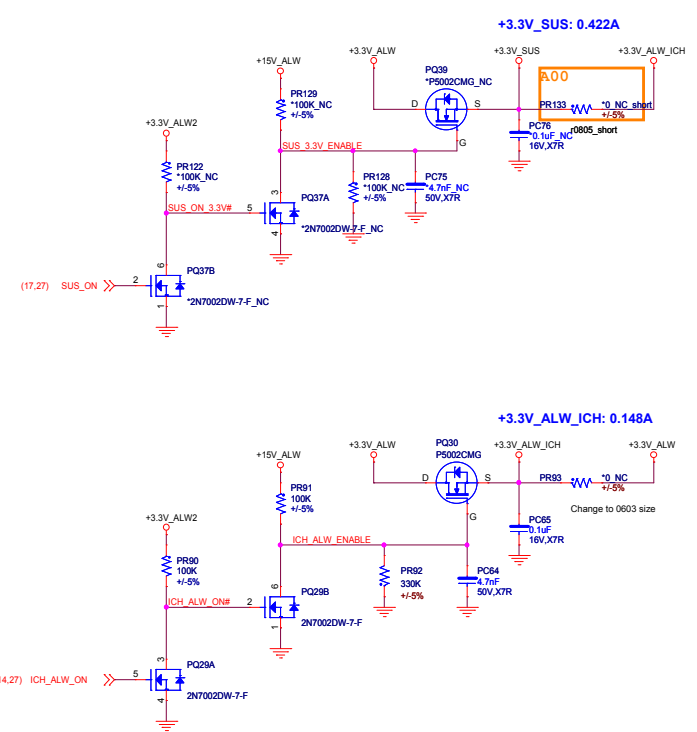
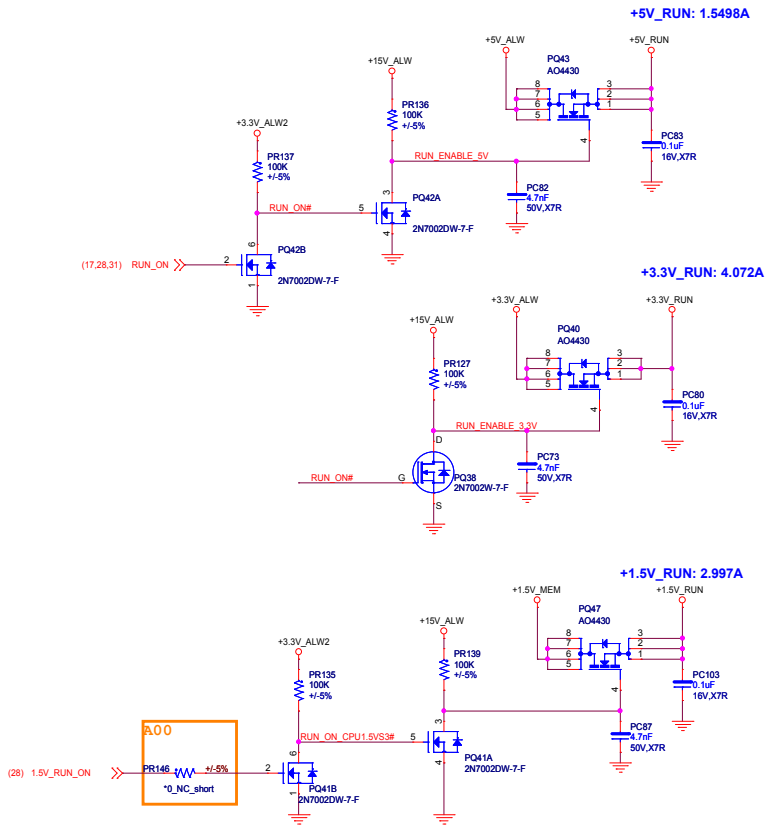
	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1



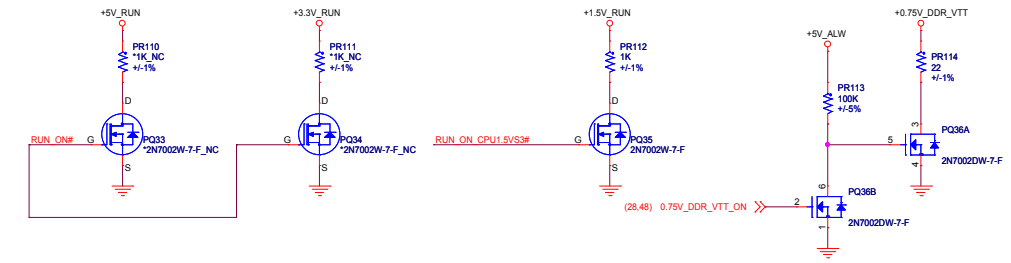
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Title		
51 -- PW_Blank for Ext.GPU		
Size	Document Number	Rev
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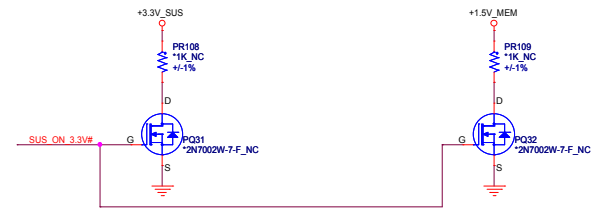


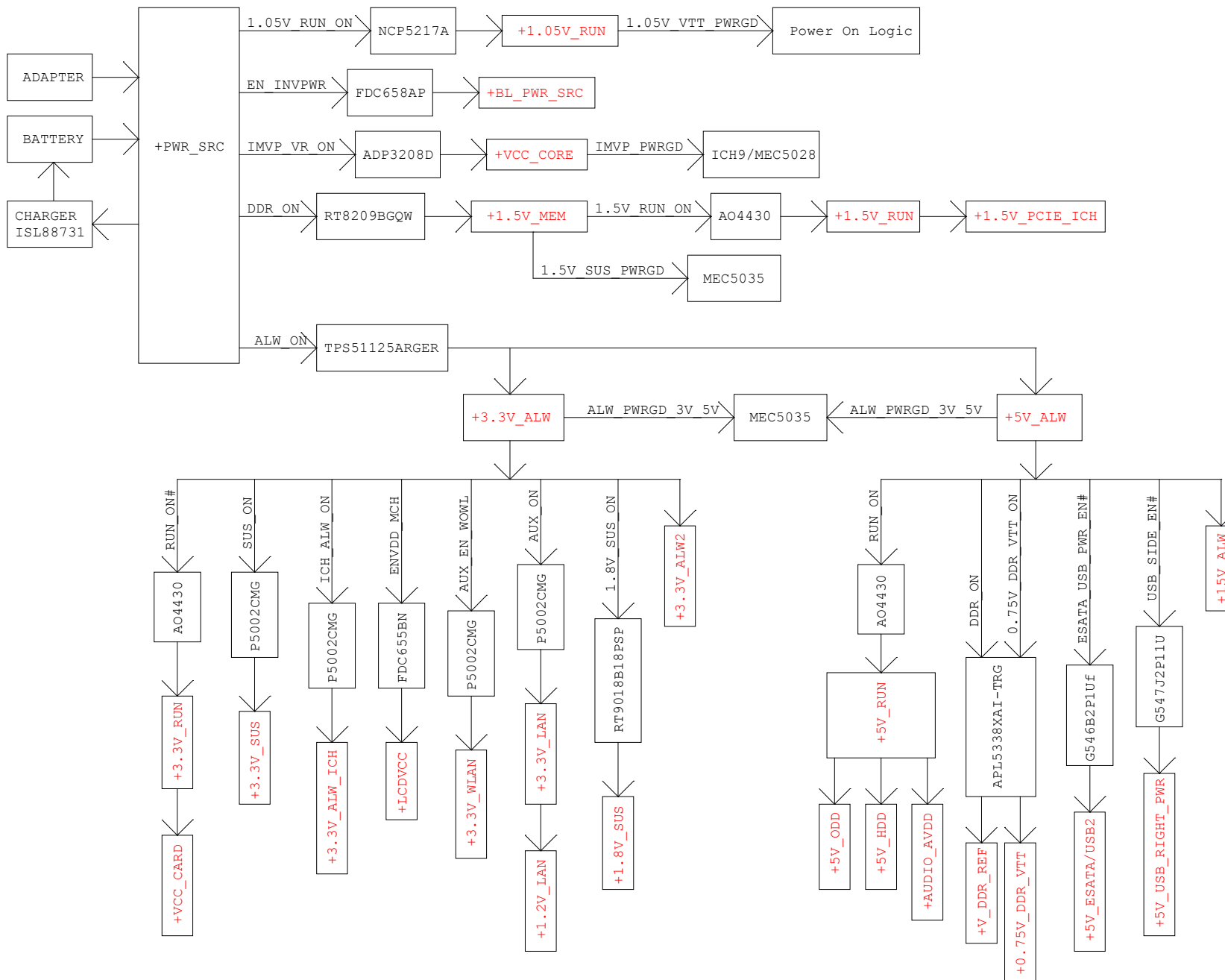


### Reserve discharge path



### Reserve discharge path



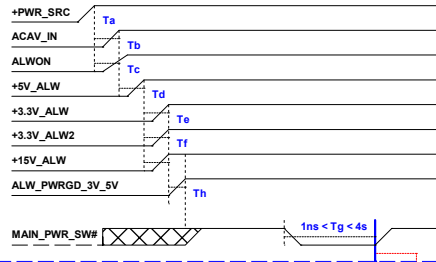




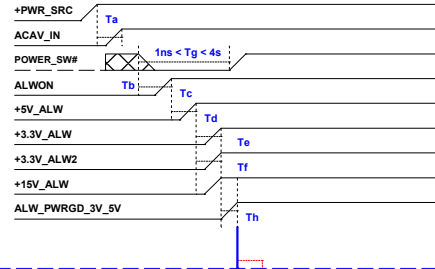




## [AC in]



## [Battery only, AC absent]



EC pay attention timing

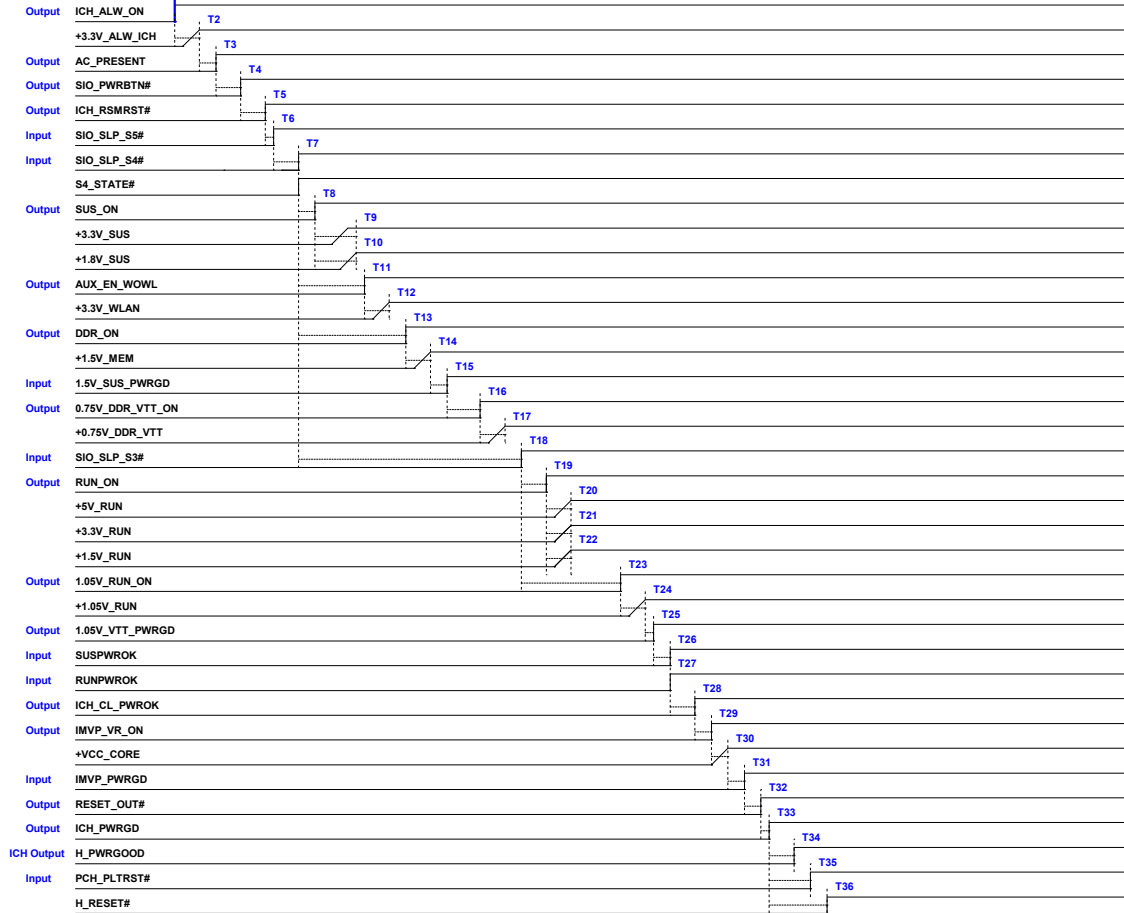
# UMA Power On Sequence

## [AC in]

ITEM	Measure Point	Time
Ta	+PWR_SRC	To
Tb	ACAV_IN	To
Tc	ALWON	To
Td	+5V_ALW	To
Te	+3.3V_ALW	To
Tf	+3.3V_ALW2	To
Tg	+5V_ALW	To
Th	+15V_ALW	To

## [Battery only, AC absent]

ITEM	Measure Point	Time
Ta	+PWR_SRC	To
Tb	POWER_SW#_MB	To
Tc	POWER_SW#_MB	To
Td	ALWON	To
Te	+5V_ALW	To
Tf	+5V_ALW	To
Tg	+5V_ALW	To
Th	+15V_ALW	To



ITEM	Measure Point	Time
T1	MAIN_PWR_SW#	To
T2	ICH_ALW_ON	To
T3	+3.3V_ALW_ICH	To
T4	AC_PRESENT	To
T5	SIO_PWRBTN#	To
T6	ICH_RSMRST#	To
T7	SIO_SLP_S5#	To
T8	S4_STATE#	To
T9	SUS_ON	To
T10	SUS_ON	To
T11	S4_STATE#	To
T12	AUX_EN_WOWL	To
T13	S4_STATE#	To
T14	DDR_ON	To
T15	+1.5V_MEM	To
T16	1.5V_SUS_PWRGD	To
T17	0.75V_DDR_VTT_ON	To
T18	S4_STATE#	To
T19	SIO_SLP_S3#	To
T20	RUN_ON	To
T21	RUN_ON	To
T22	RUN_ON	To
T23	SIO_SLP_S3#	To
T24	CPU_VTT_ON	To
T25	+1.05V_RUN	To
T26	1.05V_VTT_PWRGD	To
T27	1.05V_VTT_PWRGD	To
T28	RUNPWROK	To
T29	ICH_CL_PWROK	To
T30	IMVP_VR_ON	To
T31	+VCC_CORE	To
T32	IMVP_PWRGD	To
T33	RESET_OUT#	To
T34	ICH_PWRGD	To
T35	H_PWRGOOD	To
T36	PCH_PLTRST#	To
	H_RESET#	To

